FINAL TECHNICAL PROGRESS REPORT

ON

OPTICALLY ADDRESSABLE FERROELECTRIC MEMORY WITH NON-DESTRUCTIVE READ-OUT

TO

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EXECUTIVE SUMMARY

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Period of Performance: June '92 through January '93

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The objective of this task was to critically assess the potential of the concept of' "Optically addressed ferroelectric memory with non-destructive read-out (NDRO)" as a viable non-volatile memory technology and to identify its high impact applications. This work has clearly demonstrated the viability of optical NDRO, and identified the necessary conditions for its realization.

In particular, the highlights of this work are: (a) demonstration of high speed (-10 ns) bidirectional, polarization-dependent response at ~mW/μm^2 of incident optical power levels, (b) observation of the optoelectronic response at lower power levels preferentially from the edges of the ferroelectric capacitor suggesting the hypothesis that this effect strongly depends on the orientation of the film or a gradient of the polarization, (c)conceptualization of a device design to reduce the requirement of' incident optical power by orders of magnitude, (d) the optical NDRO signal is fundamentally different from the conventional destructive readout(DRO) mechanism, and therefore is not plagued by the problems associated with retention loss in the DRO technique, and (e) simulation of a 16 K memory chip within the framework of a radiation hard environment with read access times of $\leq$ 35 ns and read cycle times of $\leq$ 50 ns, easily surpassing those of the conventional. DRO. Commercial realization of the optical NDRO, however, would require a reduction, by about an order of magnitude, in the incident (optical) power for the readout; or an enhancement by about an order of magnitude in the delivered power/size ratio and reduction in production cost of semiconductor lasers to be used for compact implementation of the optical addressing.

l-n addition to the potential of the photoresponse as an NDRO signal., its dependence on the "product" of memory stored and incident optical signal offers opportunities for high speed optical communication networks, image processing, and parallel processing architectures such as optoelectronic neural networks.

TABLE OF CONTENTS

FINAL TECHNICAL PROGRESS REPORT

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I .In.production

Compact on-chip, radiation hard, non-volatile memory storage with high speed interactive access is desired for a wide variety of applications that need 'power-off' memory maintenance. Such applications include alternatives for battery backed defense needs and power-off memory maintenance aboard space missions. Commercial needs include data storage for intelligent automotive navigation, notebook computers, solid state voice messaging systems for telephones and pagers, and frame and configuration memory for high definition television and display systems. Ferroelectric non-volatile memories are promising for all of these applications.

With the advancement of technology to deposit thin films of PZT (lead zirconate titanate) and to integrate them with conventional silicon technology, ferroelectric non-volatile memories are now well into their development phase[1,2,3]. The memory element consists of a thin film ferroelectric capacitor, in which the non-volatile storage is based on the remanent polarization within the ferroelectric thin film. Conventional destructive readout (DRO) from a ferroelectric memory utilizes the difference signal between the charge (Q1) associated with a switching pulse and the charge (Q2) associated with a non-switching pulse. However, such a process destroys the stored information, which necessitates a rewrite operation after every read cycle. This complicates the hardware and shortens the effective life of the memory. DRO is destructive and also sensitive to bit upset at the refresh instant. Furthermore, the selection of a reference in the design of a DRO digital ferroelectric memory is non-trivial. This often occurs due to the variability of the charge Q2 as a function of the device process history, device operation history, temperature cycling and retention time. A non-destructive readout (NDRO) technique is therefore required.

An electrical method to nondestructively read the memory is with a ferroelectric field effect transistor. It relies on the modulation of the source-to-drain current, across a variable resistance semiconductor channel or semiconducting thin film, by the polarization (memory) in the ferroelectric layer and thus serves as the NDRO. Although nondestructive to the memory, this

scheme[7] involves the challenge of optimizing a new interface. In prior implementations, the ferroelectric semiconductor interface has "been plagued by non-separability of the effects of fast ferroelectric switched polarization from other spurious effects. These effects, such as injected space charge, contribute to the modulating field **and** retention loss due to leakage associated with the interface. Recently[3,9] some effort has been put into such a NDRO memory, using Barium magnesium fluoride, $BaMgF_4$ and bismuth titanate, $Bi_4Ti_3O_{12}$ as the ferroelectric thin films. However, poor retention, for just a few hours or less than half a day, respectively, have been reported.

On the other hand, the concept of an optically addressable NDRO utilizes state- of-the-art ferroelectric capacitor memories based on lead zirconate titanate materials with demonstrated retention of over several years. The concept of the optical NDRO readout consists in reading the polarization dependent photoresponse from the capacitor. When the wavelength of the incident radiation is less energetic than the bandgap of the PZT material the stored memory state is not altered. This non-destructive feature makes it a very attractive option for the niche applications of critical data storage. In addition, such a non-destructive readout (NDRO) may allow use of the ferroelectric capacitor as a nonvolatile analog memory. The constant memory refresh required in the conventional destructive readout (DRO) does not sustain the bit level precision required for an analog memory operation.

In a preliminary study we recently[4,5] observed high speed, bidirectional, polarization dependent photoresponse at a wavelength of 532 nm from ferroelectric thin film memory capacitors. This exhibits[6] potential for a high speed optically addressable non-destructive readout of the memory. Given such a high speed, bidirectional, polarization dependent response, the objectives of this task was to critically assess its potential as a viable memory technology.

II Objective

The overall objective of this research program was to develop optically addressable ferroelectric nonvolatile memory. The specific objectives of this study phase, motivated by JPL's recent feasibility demonstration of the optically addressed, high speed, nondestructive-readout of the state of remanent polarization in thin PZT films, were to:

I.Critically assess the potential of the concept of 'Optically addressed ferroelectric memory (OA-FeM) with non-destructive read-out" as a viable memory technology (for selected applications) ,

2.Project OA-FeM performance capabilities (density, read/write speed, power requirements) , and

3. Identify the necessary conditions for the realization of this technology for selected high impact applications and generate a road-map for the same.

Details of the technical progress are presented below.

III Technical Progress

In order to determine the technological viability of the optically addressable memory with NDRO, we have initially focussed on the conventional Pt/PZT/Pt - sandwich device configuration, with a nominal. goal of a 16 K memory chip design. To address this task the following subtasks were performed:

1. Computerized Multiprobe Test Assembly:

A computerized multiprobe test setup including a new laser was assembled to allow a study of the high speed photoresponse and comparison of the optical. NDRO results with the conventional DRO technique (Schematic shown in fig. la and fig. lb) . This set-up allows measurement and recording of optical NDRO behavior of the ferroelectric capacitor, along with conventional electrical DRO signal, Sawyer/Tower hysteris loop, capacitance, and resistance / leakage, etc; on the same sample without disturbing the probes. This highly integrated setup is quite flexible, versatile, interactive, and allows convenient computer storage and analysis of the data. In particular, the flexibility of subjecting a sample to the various probes, repeatedly, in any selected sequence, with a verifiable guarantee that the sample has not been irreversibly altered during the course, is extremely valuable in correlating the various phenomena studied. A small (12" long) laser in conjunction with a variable attenuator is integrated within the setup. The FWHM of the available laser pulse is as short as 6 ns.

2. Device Fabrication and Photoresponse Investigation:

A variety of device test structures in the sandwich configuration were fabricated using sol-gel thin films with platinum as top electrode. The thickness of the top electrode was as low as 100 Å to obtain semitransparent electrodes and upto 3000 A to obtain opaque, reflecting top electrodes. The photoresponse results from the semitransparent and opaque top electrodes were compared and have been documented in Ref 4. The results suggest

that at power levels greater and of the order of 20 mW/μ^2 the response is hi-directional and polarization dependent response due to a thermally triggered mechanism. In the following, we present a memory design developed based on this response and the estimated power requirements and projected performance levels for the basic sandwich device (configuration A) as well as for a modified device structure (Configuration B) with a different top electrode, which would significantly enhance its optical absorption characteristics.

In addition, our recent results on the optoelectronic effects observed already at an order of magnitude lower power levels (- 2 mW/μ^2) in the PZT samples have led to a conceptualization of a totally new device structure (configuration C) , which may have potential for dramatically improving the device performance at remarkably low intensity levels, making it an excellent candidate for further investigation. Highlights of our recent results leading to the device configuration C are also presented in Appendix A.

3a. Memory Cell design:

Starting with the known[4] photoresponse characteristics, a model memory cell design has been conceptualized. At present, a single ferro-capacitor cell design is preferred over the two capacitor differential signal sensing design for smaller cell size as well as faster access. The bidirectional nature of the response allows this flexibility. We have adapted a typical DRAM design without refresh that utilizes standard balanced bit line techniques for the bit differentiation based on the photoresponse input signal. A block diagram and schematic of the configuration is shown in Figure 2a. Fig 2b is a schematic of the typical column read functional circuit. In order to evaluate trade-offs in speed and size quickly, a Microsoft Excel worksheet was generated. To build such a worksheet, several areas of the actual design had to be simulated or designed. SPICE simulation programs were developed that allow a quick estimation of the performance parameters of the sensing circuit. The calculations and speed figures are based on simulated and measured data for existing RAM designs using a two balanced lines per bit design. The analysis can be divided into three categories: (1) Ferroelectric cell (f'cell) model, (2) Support circuitry timing and (3) Support circuitry area.

Ferroelectric Cell Model:

Utilizing the typical photoresponse data (reference 4), we have modeled the ferroelectric capacitor as a current generator with estimated constants of capacitance $C_f \sim 0.4$ $pf/\mu m^2$ and current $I_f \sim 0.32$ $\mu A/\mu m^2$. In order to perform area calculations and determine initial' initial bit line capacitance, it was necessary to produce a prototype layout of the cell. A conservative assumption was made that the ferroelectric cell could be placed within 2 minimum

dimensions of other structures in a 1.2 μ CMOS process. Furthermore it was assumed that the ferroelectric capacitor is constructed of two overlapping layers, each immediately contactable from metal one. Also it is assumed that the illumination rise times and durations are available that lead to current waveforms with rise times on the order of 1 ns or slower "and durations on the order of 10 to 100 ns. A summary of all the important assumptions made in performing this memory simulation are provided in Appendix B.

Support Circuitry Timing :

The support circuitry timing must account for the following delays. The primary delays are:

(1) Bit-line delay, T_b: The time for voltage on the bit line to reach a nominal value V_b. V_b is the minimum differential voltage required to activate the comparator and is chosen with consideration for the noise environment, the typical offsets of the bit line comparators, and the minimum expected current capability of the ferroelectric capacitor.
(2) Comparator delay, T_c: Time taken by the comparator to make a decision.
(3) Other peripheral electronic timing delays, T_e: Setup, Addressing and Multiplexing.

Bit-line Delay, T_b:

The f'cell driving various capacitances of a bit line through a small address enable N-channel MOSFET was simulated in SPICE. The simulations were performed for various sizes of the MOSFET, various sizes of the f'cell, and various loads. The time T_b in ns, to charge the bit line capacitance C_b in pF, to a value of V_b in mV, with a f'cell of self capacitance C_f in pF, and the current capability of I_f in μA, is approximated by:

$$T_b = \frac{(C_f+C_b)(V_b)}{I_f}$$

Because of the high currents available in the MOSFET, and the large self-capacitance of the f'cell, MOSFET devices larger than the minimum size of 1.2μm x 3.8μm do not appreciably affect the time for the f'cell to charge the bit line capacitance.

Comparator Delay, T_c:

Since the f'cell has a transient response to the pulse of light, the cell's effect on the bit line must be captured at a specific time. This dictates the use of a clocked comparator. Also, in order to reliably sense the difference between the two bit lines (bit and bitbar) along a column, some minimum overdrive is required to overcome the substrate gradients affecting the circuits, and the general noise and

supply line bounce associated with real systems.

In order to generate an equation for T_c, we simulated overdrives for a variety of comparators including as two extreme possibilities, a slow comparator with high noise immunity and a fast comparator with low noise immunity. For such comparators, an approximation of T_c, in ns, versus overdrive V_{OD} in mV, in the region where $V_{OD} << V_{TH}$ is

$$T_c = \frac{K_c}{\sqrt{V_{OD} - V_{ODmin}}}$$

In this case KC is a delay constant calculated from the simulated results, and V_{ODmin} is the smallest overdrive that causes the comparator to switch, in mV.

Other Time Delays, T_e:

Other peripheral electronic timing delays include:

(1) the time to drive the address lines and enable one ferro-capacitor onto each column,
(2) the additional delay to multiplex the requested columns/bit into one bit and
(3) the setup time to register the output

The total access time is a summation of all these three individual time delays.

$$T_{access} = T_b + T_c - t\ T_e$$

Further to obtain the read cycle time, T_{cycle}, the additional time to re-balance, or precharge, $T_{precharge}$, the bit lines is then added to the above evaluated read access time.

Support Circuitry Area:

The area of the f'cell support circuitry, mainly the address enable MOSFET, is used to allow calculation of the area of the core for various memory configurations. Additional support circuits were not designed or simulated for timing since it was presumed that unconstrained area and drive capability is available outside the periphery of the core itself. None of the requirements for drive or timing are difficult to achieve in a modern 1.2μm process, and infact, the requirements imposed by the f'cell design used here are quite similar to conventional DRAM.

The results of a typical worksheet run are exhibited in Table I. In addition to the results for a 16K chip, the worksheet also shows the simulated results for a 64K chip.

3b. Radiation considerations for Ferroelectric Memory Readout Electronics:

The simulation framework that is being utilized provides the generic design parameters for the memory. If the application requires a radiation hard chip, the" fabrication process could be selected such that it provides hardness out to 1 Mrad total dose exposure.

Exposure to radiation over a sustained period of time (total dose) will modify the behavior of the transistors and degrade their performance. The n-channel threshold voltage gets smaller and the p-channel thresholds get larger, mobility is reduced, and leakage current increases. If the exposure is large enough, the circuits will fail completely because the n channel transistors cannot be turned off and the p channel transistors cannot be turned on. Before this failure occurs the circuit will experience a reduction in speed due to the changes in voltage threshold and carrier mobility. However, circuits processed utilizing a rad-hard process will not experience degradation until very large doses are encountered (> 1 MRad) .

'l'he simulations described here have been based on a commercial. process that is available through MOSIS. These processes are not designed for a high radiation environment. They are typically good for ~ 10-50 KRads before serious degradation occurs. With nominal operation conditions a read access time of < 20ns could be obtained using such a process with minimum feature sizes of 1.2 μm. Lowering the feature size to 0.8 μm will entail further improvement in speed. Using data obtained from experiments conducted on the CRRES satellite, and considering an example where a 20-30 KRad total dose impingement was done on the circuits, a speed degradation of between 2 to 2.5 times was projected. This degradation was applicable to times T_c and T_e. Using this modificati on the simulation yielded an increase in access time from 19 ns to 34 ns to allow for a margin for radiation hardness. If instead a Rad hard (> 1 Mrad) process were to be used it would give similar speed range in its operation upto the specified 1 MRad limit.

4. Identification of Memory Requirements for selected applications:

Requirements of five different selected groups of users are summarised as follows:

1. SDIO's missile interceptor (possible high radiation),
2. Aerospace surveillance satellites (rugged, intermediate lifetime ~ 5 years) ,
3. Defense critical data storage (compact, portable, some frequent write/read operations),

4. Power-off memory maintenance onboard NASA's deep space missions (long lifetime, over 10 years retention), and
5. Automotive industry (vibration and temperature immune)

As far as readout is concerned, the most stringent requirements came from the SDIO users: a read access time of ~ 150 ns and read cycle time ~ 200 ns for an NDRO NVM). Indeed, projected readout performance of our optical NDRO promises to be almost an order of magnitude better.

5. Retention, Comparison DRO & Optical NDRO:

Recently[10-12], it has been recognized that the bit errors in conventional DRO device primarily depend on Q2 (the charge associated with the non-switching pulse during readout) rather than Q1 (the charge associated with the switching pulse). A gradual rise in Q2 with time, generally attributed to time dependent depolarization and slow switching polarization components, has an apparent effect of eroding the magnitude of the readout signal. The time dependent polarization components may have their origin in thermally activated switching, slowly reorienting space charge in traps/grain boundaries, a distribution of non-oriented grains, unstable domains, and/or slow domain kinetics with high nucleation barriers.

Figure 3 shows a comparative plot of polarization and photo-response as a function of retention time, as measured by the DRO technique and the optical NDRO technique for the as-deposited and post top electrode deposition anneal (PTEA) treated capacitors. The two characteristics are very similar for the PTEA capacitors. However, for the as-deposited capacitors, the NDRO characteristics are markedly stable, whereas the DRO characteristics exhibit a rapid retention loss due to the increase in Q2 with retention time. This suggests that the NDRO reflects mainly the variation of charge associated with the switching pulse, Q1, and is quite independent of the effects that cause Q2. This implies that the problems associated with conventional DRO due to Q2 variability will be nonexistent in the optical NDRO technique. Thus, the optical NDRO, in addition to being non-destructive, promises a more reliable operation of the non-volatile memory.

6. Power requirements study:

Device Configurations

Device Configuration A (figure 4) refers to the conventional Pt/PZT/Pt sandwich structure. Our current VLSI design for a sense amplifier for 16 k memory chip requires ~ 40 mV signal to be able to unambiguously read a bit. Therefore, to generate that level of signal, with an optical pulse of ~ 10 ns duration, projections from our NDRO observations for a nominal capacitor area of ~ 20 μm^2)

result in:

** read access time ~ 20 ns (Spice simulation result, no rad-hard margins)
< 35 ns (extrapol.ation w/ rad-hard margin)

** read cycle time - 30 ns (Spice simulation result, no rad-hard margins)
< 50 ns (extrapolation w/ rad-hard margin)

** chip power consumption < 1 Watt

i. Although the access speed projected above is competitive and offers an edge over other NVM memory technologies, such a device would reguire -400 mW peak optical power/capacitor or ~ 20 $mW/\mu m^2$ of power to area] size ratio is required for the optical NDRO read operation. Compact semiconductor lasers in that power range are not available at present time. Commercial semiconductor lasers are available that can deliver ~ 0.01 $mW/\mu m^2$. Additionally devices demonstrated in the laboratory with ongoing R& D efforts have shown13 to deliver - 0.1 $mW/\mu m^2$.

ii. Alternatively, diode laser pumped solid state lasers along with an acousto-optical scanning system may be packaged in a size of ~ (10 x 6 x 6) cm^3 implementation along with a electronic circuitry box of the size of a cube of 10 cm on each side. However, the scan rate will limit the read frequency to about **a** Megahertz and the wall plug power requirement for such a package will exceed 10 watts!

Device Configuration B: (figure 5) is essentially the same sandwich device described above except for replacement of the highly reflective platinum top electrode (optical absorptivity ~1%) by a better absorptive layer (say, platinum cermet film with an absorptivity in excess of -80%) It will clearly reduce the required peak power per pixel to below ~ **0.5** $mW/\mu m^2$, however even that needs to await about an order of magnitude enhancement in the power to size ratio in order to allow a compact implementation (figure 6) as a dual chip with a flip bonded semiconductor laser chip onto the ferroelectric chip.

Also in this thermally triggered read mechanism, however, the read access cycle time for the same bit would be as long as a fraction of a microsecond, due to the extended oppositely directed relaxation observed[4] in the photoresponse.

Device Configuration C is based on our recent observations (appendix A, figure 7) of the opto-electronic effect. The conceptualized device would consist of a planar geometry (Figure 8) where PZT would be deposited with its c axis parallel to the substrate plane, and the two metal electrodes used for write as well as read operations would touch the two facing edges of PZT. This would utilize the polarization dependent photoresponse

(Appendix A, figure 9a and 9b), already observed at an order lower optical incident energy (- 2 $mW/\mu m^2$), as a bidirectional measure of the polarization state of the memory.

In the following are outlined the features of the new configuration that promise its lower power requirement (lowering by about two orders of magnitude) and potential for ready manufacturability:

i. Our observation of photoresponse from the conventional sandwich structure suggests that the response is primarily from the narrow "edge" regions of PZT surrounding the circular, opaque top electrode. Clearly, the bulk of PZT with remanent polarization (memory), which is totally covered by the top electrode, does not even get "addressed" by the incident light. The observed response therefore could be attributed mainly to only the weakly polarized regions of PZT in the edge regions. This was further confirmed by moving around the beam spot across the top electrode both in case of semitransparent or opaque top electrodes, and the response was seen to originate mainly from the edges. Moreover, the direction of the polarizing field in the edge region, moving away from the edge of the top electrode, does not remain normal to the plane of the film. This suggests that the polarized domains contributing to the photoresponse may be from the smaller population of non-c-axis oriented domains (tilted and therefore aligned with the polarizing field direction in the edge region).

The proposed device with the planar geometry would allow ease of polarization of PZT in the planar (c-axis) direction with two distinct polarity options. Furthermore, the incident light beam would illuminate (and therefore address) the full area of active, polarized PZT for dramatically increased signal (atleast by one order). This configuration is similar to the one studied by Bass and others[14-16] in a variety of ferroelectric single crystals to observe the optical rectification effect.

ii. The new configuration will allow an optimum[12] 90° incidence of the optical beam thus giving another factor of 20% to 30% over the currently measured value.

iii. From reports[16] on work done on single crystals a dependence of the photovoltage on optical polarization state of incident beam is known. The initial measurements on PZT films, with the c axis in the plane of the substrate, in the new configuration will allow rigorous computation of the electrooptic coefficients and thereby allow a more exact projection of the desired optical polarization to maximize the photoresponse voltage.

iv. single level of contact metallization required

7. Compact **Implementability** of Device configuration B or C in a **power** competitive manner:

Desired/Acceptable Wall Plug Power: 1-2 **W**

We have previously (Figure 6) suggested the architecture of a dual ferroelectric-laser chip pack where the laser chip is flip bonded on top of the ferro-chip. The ready manufacturability of such a chip design in a compact dense packed manner relies completely upon bringing the power requirement down to about 0.1 mW/μm or less so that demonstrated laser technologies (VCSEL technology with individual row addressability) may be utilized with -1-2 W of wall plug power to build such an optically addressable chip. The optoelectronic effect observed is clearly the most promising to pursue further in order to achieve this goal because it has the potential of reducing the power required by another couple orders of magnitude and thereby may surpass the desired goal .

At the cost of more real estate due to looser packing density and an order of magnitude more wall plug power, the chip pack may be implemented more immediately (Figure 10) using monolithically integrated bars of edge emitting lasers which have been made surface emitting by etching 45° mirrors or diffraction grating. With the current requirement of about 40 mW of peak power per pixel in a 16K architecture a wall plug power of about 15 W will be required. On the other hand having achieved the desired goal of 0.1 mW/μm^2, the wall plug power demand from this architecture as well would drop to ~ 2 Watts making it very manufacturable and competitive with the other NVM technologies.

In addition to its promising prospects for NDRO, the optoelectronic effect has further potential for replacing a combination of a spatial light modulator and a detector in the backplane of optical computers by a single compact device array as it offers to be a programmable detector within one single array. This potential emerges because of the dependence of the photoresponse on the "product" of memory stored and incident optical signal. Such functionality from an integrated device, by reducing the size and complexity of the implementation and enhancing the speed by allowing parallel access, offers opportunities in a wide spectrum of applications including high speed optical communication networks, image processing, and parallel processing architectures such as optoelectronic neural networks.

8. **Deposition of PZT with c-axis parallel to the substrate plane:**

Using a suitable template layer such as MgO and selection of the growth conditions (substrate temperature and ambient partial pressure) polycrystalline/epitaxial films with preferential a axis orientation can be deposited as has been demonstrated in the case

of YBCO[17], $BaTiO_3$ [18] and $PbTiO_3$ [19]. Therefore the new conceptual design **C is** indeed capable of being realized within **a** future R & D program.

IV Conclusions and a Road-Map for Future Development

This work has clearly demonstrated the feasibility of optical NDRO, and identified the necessary conditions for its realization.

In particular, the highlights of this work are:

(a) demonstration of high speed (-10 ns) bidirectional, polarization-dependent response at -mW/pm* of incident optical power levels,

(b) observation of the optoelectronic response at lower power levels preferentially from-the edges of the ferroelectric capacitor suggesting the hypothesis that the effect strongly depends on the orientation of the film or a gradient of the polarization,

(c) conceptualization of a device design to reduce the requirement of incident optical power by orders of magnitude based on utilizing the optoelectronic effect,

(d) the optical NDRO signal is fundamentally different from the conventional destructive readout(DRO) mechanism, and therefore is not plagued by the problems associated with retention loss in the DRO technique.

(e) simulation of a 16 K memory chip within the framework of a radiation hard environment with read access times of $\leq$ 35 ns and read cycle times of $\leq$ 50 ns, easily surpassing those of the conventional DRO.

Commercial realization of the optical NDRO, however, would require either a reduction, by about an order of magnitude, in the incident (optical) power for the readout; or an enhancement by about an order of magnitude in the delivered power/size ratio and reduction in production cost of the semiconductor lasers to be used for the optical addressing. It is interesting to note that at the time this report was being compiled, a news item[20] from **AT&T Labs reports the achievement of a ten-fold increase in output power to size ratio delivered from VCSEL to about 1 mW/μm^2 at a wavelength of ~ 0.8 μ, thus making the compact implementability power-wise feasible already.**

The further R&D to convert this optically addressable ferroelectric memory technology into a viable product therefore requires a focus on primarily the following items:

1. Investigation of the optoelectronic response to verify the hypothesis for the origin/mechanism of the observed interesting photoresponse from the edges.

2. Development of the new device design conceptualized herein to realize the full potential of the optical NDRO technology towards the identified high impact applications in optical computing and high speed communications.

3. Successful, reliable and cost effective integration of the ferroelectric technology with the conventional. VLSI Technology and the optical addressing options such as semiconductor lasers, optical fibres and/or image projections using lenslet arrays. In this respect the optically addressable ferroelectric technology may have a substantial advantage over the conventional electrically addressable ferroelectric technology because of considerably reduced peripheral circuitry requirement owing to the parallel access needed for optical processing applications.

V. Additional Accomplishments.

In addition, this program also led to the following:

1. Identification of time dependent polarization effects in PZT films and their reduction by an optimized anneal treatment,

2. a new concept of a non-invasive optical probe for studying / mapping the remanent polarization profiles / ferroelectric domains in PZT films and other similar ferroelectric materials with a high spatial resolution, and

3. a potential use of high band gap perovskite titanates (e.g. PZT) for UV sensing.

References:

1. D. Bondurant and F. Gnandinger, IEEE Spectrum, 30 (1989).

2. J. F. Scott and C. A. Paz De Araujo, Science, 246, 1400 (1989).

3. S. Sinharoy, H. Buhay, D. R. Lampe and M. H. Francombe, J. Vat. Sci. Technol. A, 10, 1554 (1992).

4. S. Thakoor, Appl. Phys. Letters 66, 3319 (1992).

5. S. Thakoor, J. Perry and J. Maserjian, Proc. of the Fourth International Symposium on Integrated Ferroelectrics, March 1992, Monterey, CA (to be published).

6. S. Thakoor, Proc. Second European Conf. on Polar Dielectrics, London, April 12-15, 1992.

7. S. Y. Wu, IEEE Trans. Electron Devices ED 21, 499, (1974).

8. K. Sugibuchi, Y. Kurogi and N. Endo, J. Appl. Phys. 46, 2877 (1975).

9. S. Sinharoy, H. Buhay, D. R. Lampe and M. H. Francombe, presented at International Symposium on Applied Ferroelectrics, Greenville, South Carolina, August 31-September 2, 1992.

10. S. Thakoor, "slow switching polarization component in ferroelectric thin film capacitors", ISIF-91.

11. M. Lakata and S. Thakoor, "Pulse testing of ferroelectric thin film capacitor", ISIF-92.

12. S. Thakoor, "Optically addressable ferroelectric memory", ISAF-92.

13. R. A. Morgan, K. Kojima, T. Mullally, G. D. Guth, M. W. Focht, R. E. Leibenguth, and M. Asom, Appl. Phys. Lett. **61, 1160,** 1992; A. Von Lehmen, C. Chang-Hasnain, J. Wullert, L. Carrion, N. Stoffel, L. Florez, and J. Harbison, Electronics Letters, 27, 583 1991; D. Mehuys, D. F. Welch, R. Parke, R. G. Waarts, A'. Hardy, D. Scifres, Electronics Letters, 27, 492 (1991).

14. M.Bass, P. A. Franken, J. F. Ward, and G. Weinreich, Phy. Rev. lett, 9, 446, (1962).

15. M. Bass, P. A. Franken, and J. F. Ward, Phys. Rev. A, 138, 534, (1965).

16. B. N. Morozov and Yu. M. Aivazyan, Sov. J. Quantum Electron. 10, 1, (1980). V. M. Nesterenko and B. N. Morozov, Sov. J. Quantum Electronics, 1, 496, 1971.

17. L.D. Chang, M. Z. Tseng and E. I,. Hu, Appl. Phys. Lett., 60, 1753, (1992); B. M.Clemens, C. W. Nieh, J. A. Kittl, W. L. Johnson, J. Y. Josefowicz and A. T. Hunter, Appl. Phys. Lett., 53, 1871, (1988).

18. K. Nashimoto, and D. K. Fork, Appl. Phys. Lett., 60, 1199, (1.992).

19. Wei-Yung Hsu and Rishi Raj, Appl. Phys. Lett., 60, 3105, (1992); B. S. Kwak, A. Erbil, B. J. Wilkins, J. D. Budai, M. F. Chrisholm and L. A. Boatner, Phys. Rev. Letters, 68, 3733, (1992).

20. C. Brown, Electronic Engineering Times. Feb 15, 1993, pg 33.

VI I Publications / Presentations resulting from this effort:

1. S. Thakoor, "Non-destructive Readout (NDRO) from Ferroelectric PZT thin Film Capacitorsil, Ceramic Transactions: Ferroelectric Films, Edited by A. S. Bhalla and K. M. Nair (Published by American Ceramic Society, Westerville, Ohio), 25, 251 (1.991)

2. S. Thakoor, A.P. Thakoor, and S. E. Bernacki, "Photoresponse from thin Ferroelectric Films of Lead Zirconate Titanate", Proc. Third International Symposium on Integrated Ferroelectrics, Pg. 262, April 3-5, 1991, Colorado Springs, Colorado.

3. S. Thakoor, "High Speed, Non-destructive Readout from Thin Film Ferroelectric Memory", Appl. phy. Lett. 60, 3319, 1992.

4. S. Thakoor, J. Maserjian, J. Perry, "An Optical Probe for Ferroelectric Thin Film Memory Capacitors", (to be published) Proc. Fourth International Symposium on Integrated Ferroelectrics, March 9-11, 1992, Monterey, California.

5. S. Thakoor, "High Speed, Optoelectronic Non-destructive Readout from Ferroelectric Thin Film capacitors" Ferroelectrics, 134, 355, 1992.

6. S. Thakoor, and J. Maserjian, "Photoresponse Probe of the space charge distribution in Ferroelectric PZT thin film memory capacitors" (to be published).

7. "High Speed, Non-Destructive Readout (NDRO) from thin Film Ferroelectric Memory", Fourth International Symposium on Integrated Ferroelectrics, Monterey, California, March 9-11, 1992.

8. "Pulse Testing of ferroelectric Thin Film Capacitors for Space Applications", Fourth International Symposium on Integrated Ferroelectrics, Monterey, California, March 9-11, 1992.

9. "Write time Dependence of polarization and Retention in Ferroelectric Thin Film Capacitors", DARPA Workshop on Ferroelectrics, Monterey, California, March 12-13, 1992.

10. "High Speed, Optoelectronic Non-destructive Readout (NDRO) from Ferroelectric Thin Film Capacitors", Second European Conference on Applications of Polar Dielectrics, Imperial College, London, U.K., April. 12-15, 1992.

11. "Optically Addressable Ferroelectric Memory with Non-destructive Readout (NDRO)", International Symposium on Applications of Ferroelectrics, Greenville, South Carolina,

Aug 31-Sept 2 1992.

New Technology Reports / NASA Tech Briefs / Patents:

1. "Ferroelectric/optoelectronic Memory/Processor", NASA TechBriefs, Vol. 16, No. 4, p. 28 (1992) .

2. "New Technique for Deposition of Ferroelectric/Piezoelectric Thin Films of Multicomponent Oxides Like Lead Zirconate Titanate and Related Derivatives by Multitarget Sequential dc Magnetron Sputtering at Ambient Temperatures," New Technology Report (March 1990) # 18221-CALTECH 7732.

3. "Hybrid Optoelectronic Processer for Pattern Recognition and Optical Computing Based on Ferroelectric Memory Array," New Technology Report (April 1990) # 18222-CALTECH 7734.

4. "Photon Beam Induced Current - a Non-Invasive Diagnostic Tool for Ferroelectric thin films and Devices" New Technology Report (April 1991) # 18549

5. "Development of a Thin Film Ferroelectric Capacitor for Improved Stable NonVolatile Memory Operation Both Digital and Analog" New Technology Report (April 1991) # 18551.

6. "Identification of Slow Switching Polarization Components in Thin Film Ferroelectric Capacitors" New Technology Report (April 1991.) # 18550.

7. "Design of a Compact Optically Addressable Ferroelectric Thin Film Memory" New Technology Report (April 1991) # 18573.

8. "High Bandgap Perovskite Titanate Based Solar Blind, Radiation Hard, Tuneable Detector" New Technology Report, September 1991 # 1.8695/8249.

9. "Automated Ferroelectric Capacitor Testing System", New Technology Report, September 1991 # 18696/8250.

10. "Ambient Temperature Sputtering of COmpOSite Oxide Films", NASA TechBriefs, Vol. 16, No. 9, p. 125 (1992).

11. "Planar Ferroelectric Non-Volatile Memory Device with Optical non- destructive Read-Out (NDRO), New Technology Report, November 1992 #19033/8614.

12. "Enhanced Fatigue and retention in ferroelectric Thin film Memory Capacitors by Post-Top Electrode Anneal treatment", patent filed (1992).

VIII Appendix A

**** Key Results, Opto-electronic Effect:

* **The key result as summarised in figure 7 consists in the observation of a polarization dependent rectification of the photoresponse** from the capacitor at an order of magnitude less power ($\sim 2mW/\mu m^2$) then is required for the thermally triggered response from conventional capacitors.

* This optoelectronic effect was observed, when the beam size was larger than the size of the capacitor.

* The extent of the rectification and the direction of rectification varied with the polarization of the incident beam and the angle of incidence. Such dependence on polarization state of the optical beam has been reported[16] earlier.

* A bidirectional response has been observed from a pair of adjacent capacitors with the beam illuminating the center area (i.e. with an A1A2 illumination is shown in figure 7).

* By moving around the beam spot across the top electrode both in case of semitransparent or opaque top electrodes, the response is seen to originate mainly from the edges. There is some similarity between this observed effect and the optical rectification effect that has been observed in single crystals[14-16] with the optical illumination perpendicular to the c axis of the crystal.

* Irrespective of the size of the beam spot as long as the power density per unit area was identical the photoresponse was identical.

IX Appendix B:

Summary of Assumptions made for the VLSI Simulation:

(1) Area and related capacitance calculations are based on Orbit 1.2 μm design rules and electrical specifications.

(2) The calculations are derived from simulations based on Level 2 SPICE model for Orbit 1.2μm process

(3) Memory peripheral timings are valid for memories in the size of 1 K to 256K bits.

(4) Ferroelectric capacitor cell illumination is unconstrained to the point of stimulating current risetimes of 1 ns or slower and current pulse durations of 10 to 100 ns.

(5) Ferroelectric capacitor layer overlap is fixed at 1.4 μm in width and is unconstrained in overlap height.

(6) The bit cell height for normalised f'capacitor of area = 0 is fixed at 14.2 pm. This can be changed to accommodate design rule changes, within the range -10% to +10% without changing accuracy of capacitance calculations appreciably.

X Figure Captions:

Figure la: Schematic of the computerized multiprobe test assembly.

Figure lb: Schematic of the optical set-up for non-destructive laser pulse probing of the ferroelectric capacitor.

Figure 2a: Block diagram of the memory chip configuration.

Figure 2b: Schematic of a typical column read functional circuit.

Figure 3: Results of a comparative retention study using the DRO and optical NDRO technique.

Figure 4: Illustration of device configuration A

Figure 5: Illustration of modified device configuration B to maximize thermally triggered NDRO response.

Figure 6: Illustration of an optically addressable ferroelectric memory - semiconductor laser dual chip pack.

Figure Summary of the key observations of the optoelectronic effect.

Figure 8: Illustration of the new device configuration C that maximizes the newly observed optoelectronic NDRO response.

Figure 9a: NDRO photoresponse signal from a ferroelectric test structure consisting of two capacitors coupled back to back. This is response from a positively poled test structure.

Figure 9b: NDRO photoresponse signal from a ferroelectric test structure consisting of two capacitors coupled back to back. This is response from a negatively poled test structure.

Figure 10: Layout of a 16K optically addressable ferroelectric chip utilizing bars of edge emitting lasers made surface emitting by etching mirrors or diffraction grating.

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SCHEMATIC OF TEST SETUP

(TO BE USED WITH THE JPL FERROELECTRIC TESTING PROGRAM, JFETP)

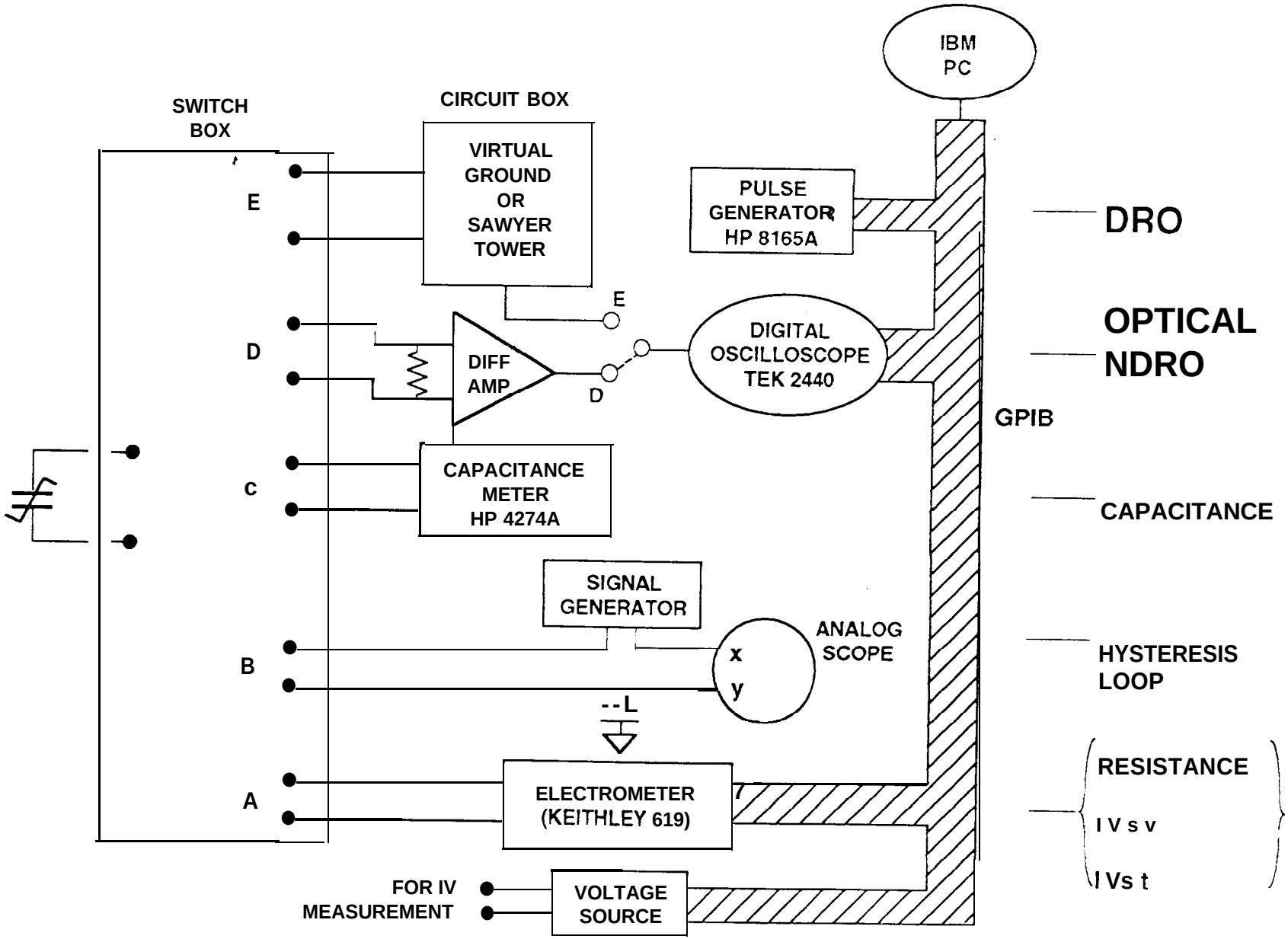

Figure 1a

NON-DESTRUCTIVE LASER PULSE PROBING OF THE FERROELECTRIC CAPACITOR

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SCHEMATIC OPTICAL SET-UP

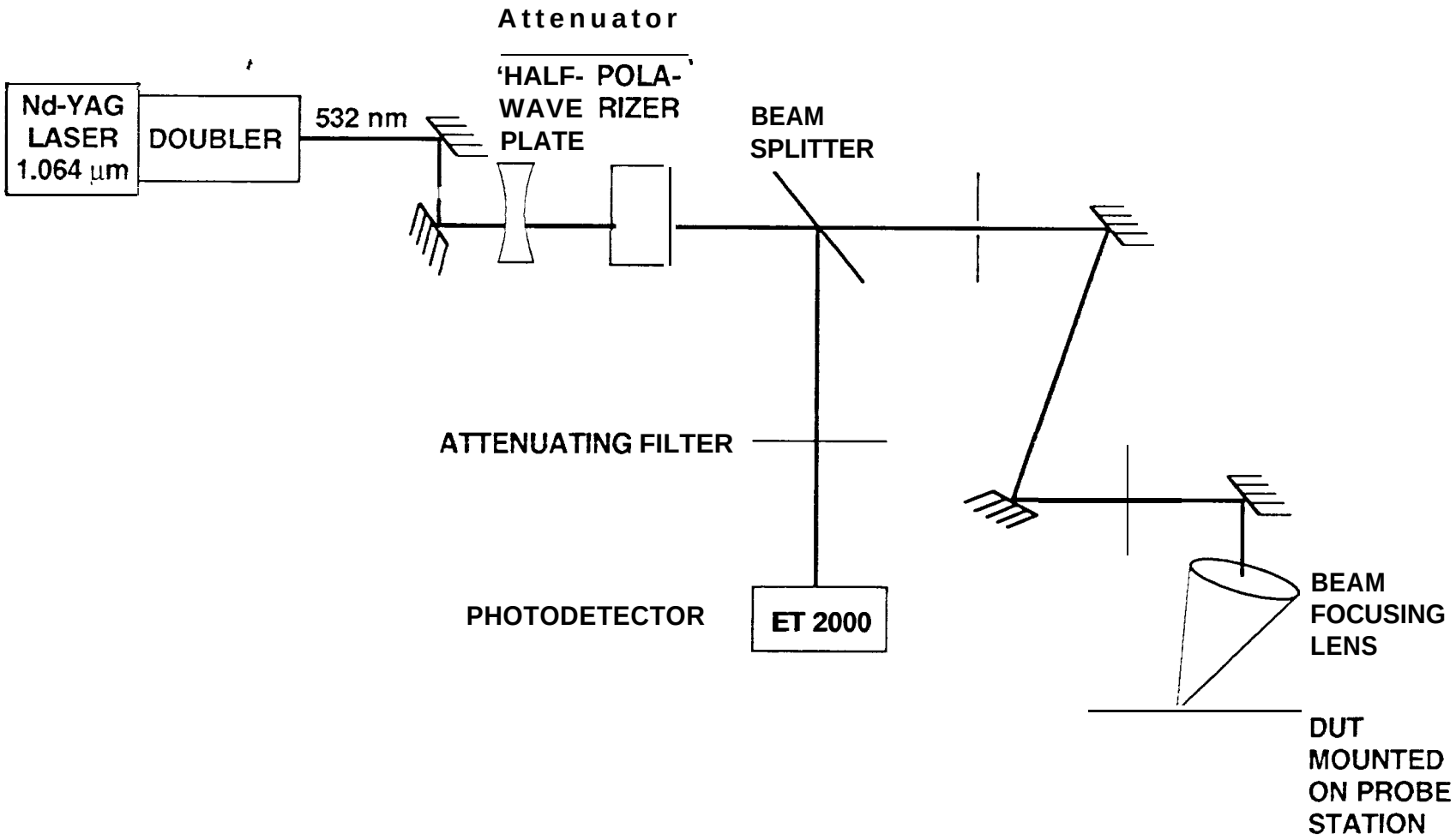

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Figure 1b

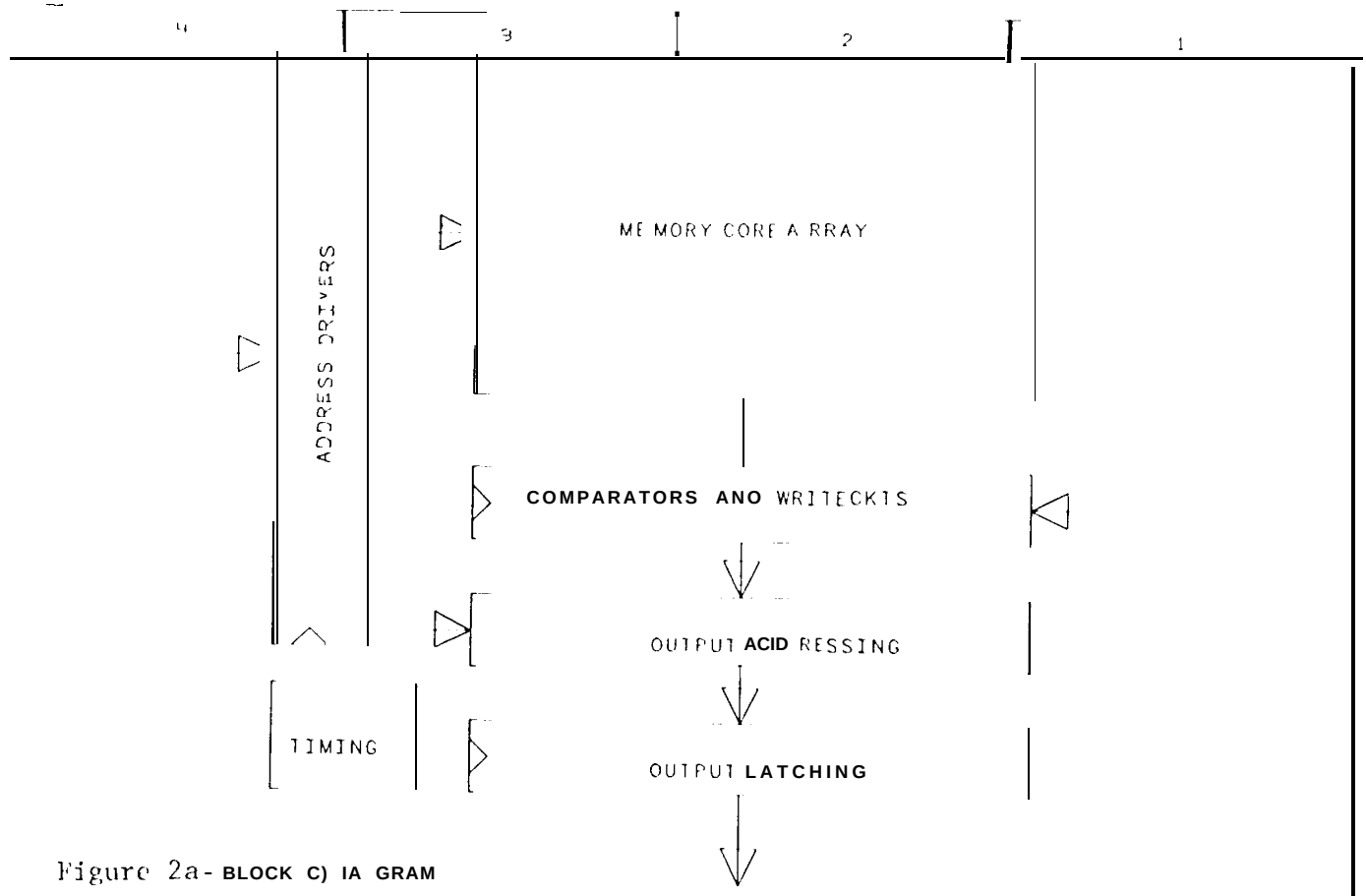
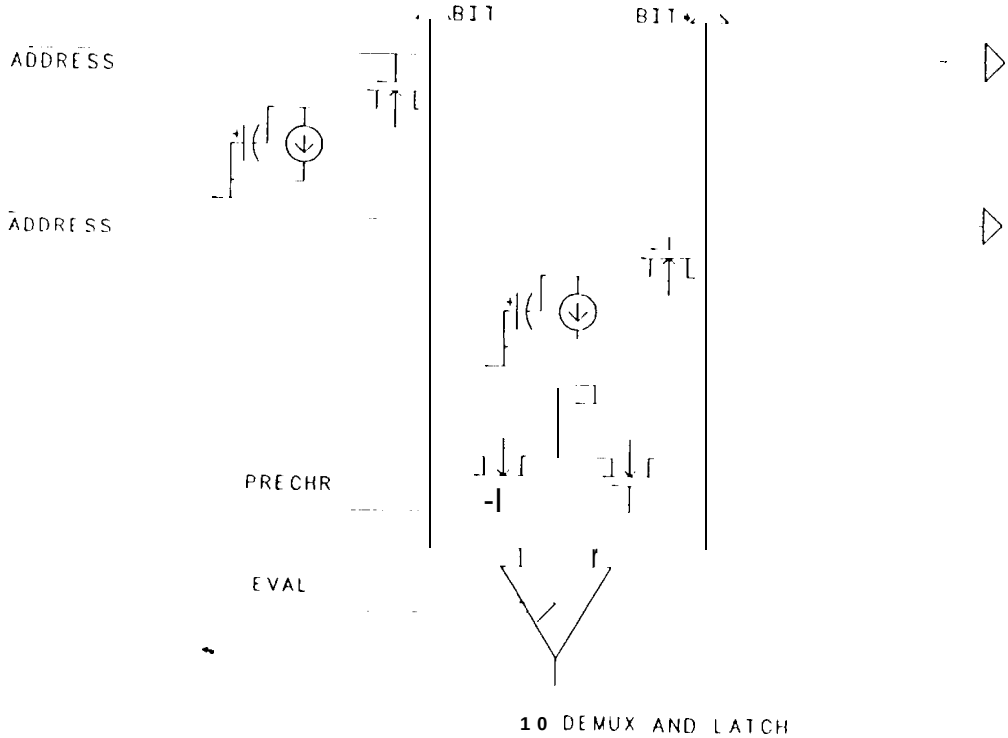


Figure 2a- BLOCK C) IA GRAM



igure 2b COLUMN READ FUNCTIONAL CIRCUIT

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		ENGINEER:	PAGE:

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COMPARATIVE RETENTION STUDY
DRO AND OPTICAL NDRO

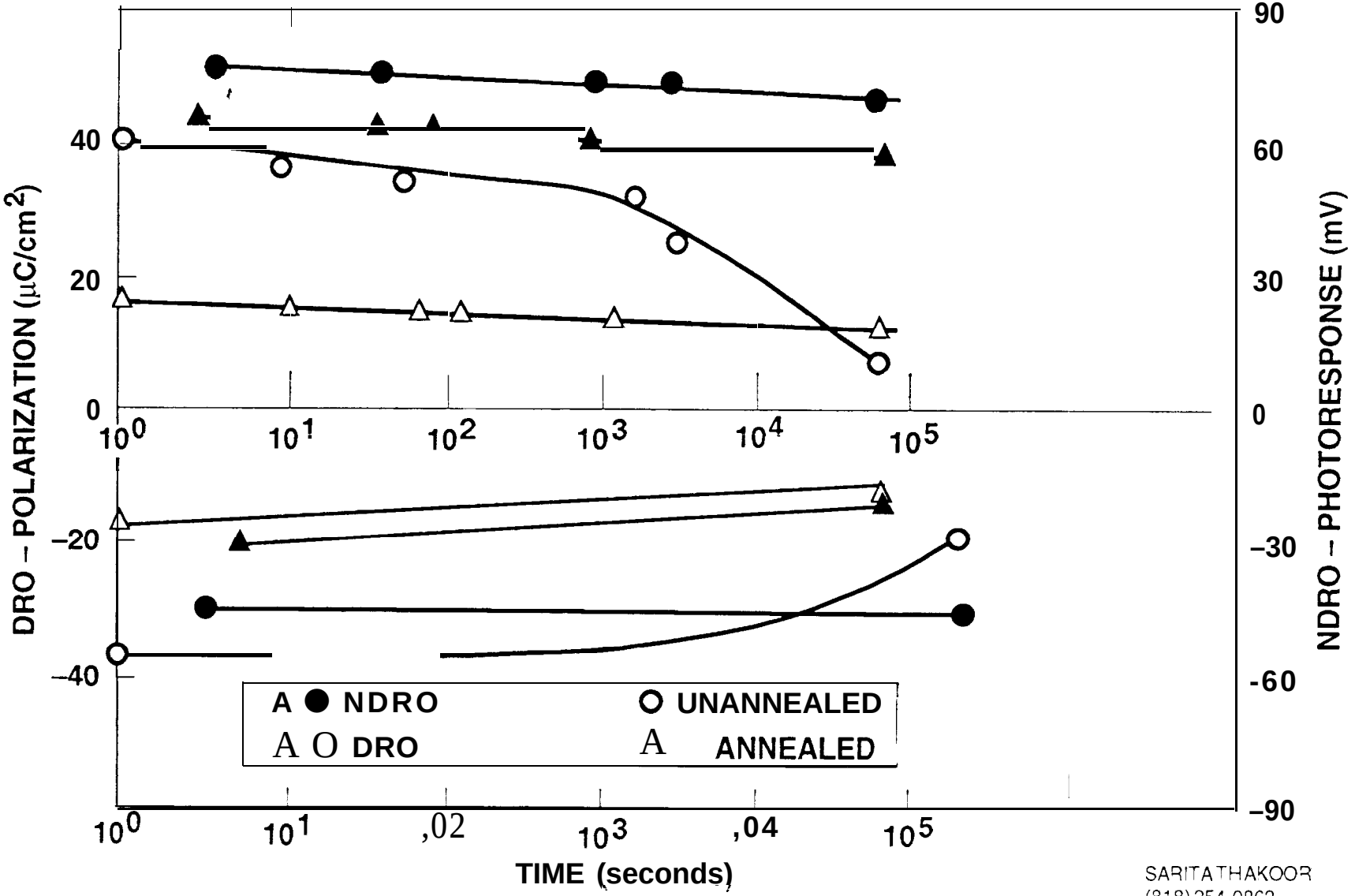

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Figure 3

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FERROELECTRIC THIN FILM CAPACITOR DEVICE CONFIGURATION A

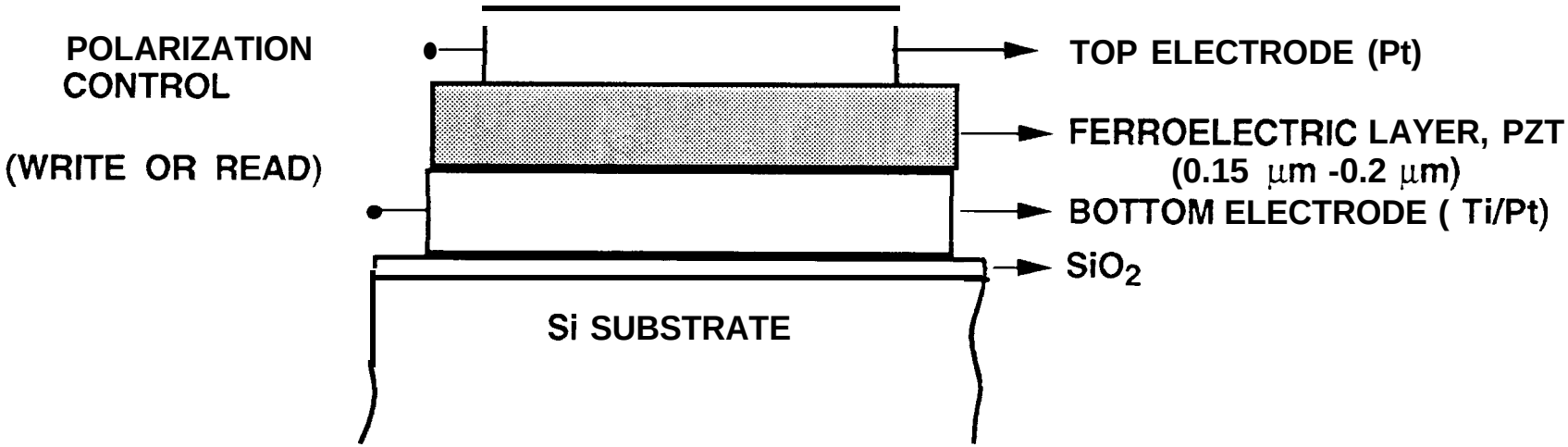

Figure 4

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DEVICE CONFIGURATION B

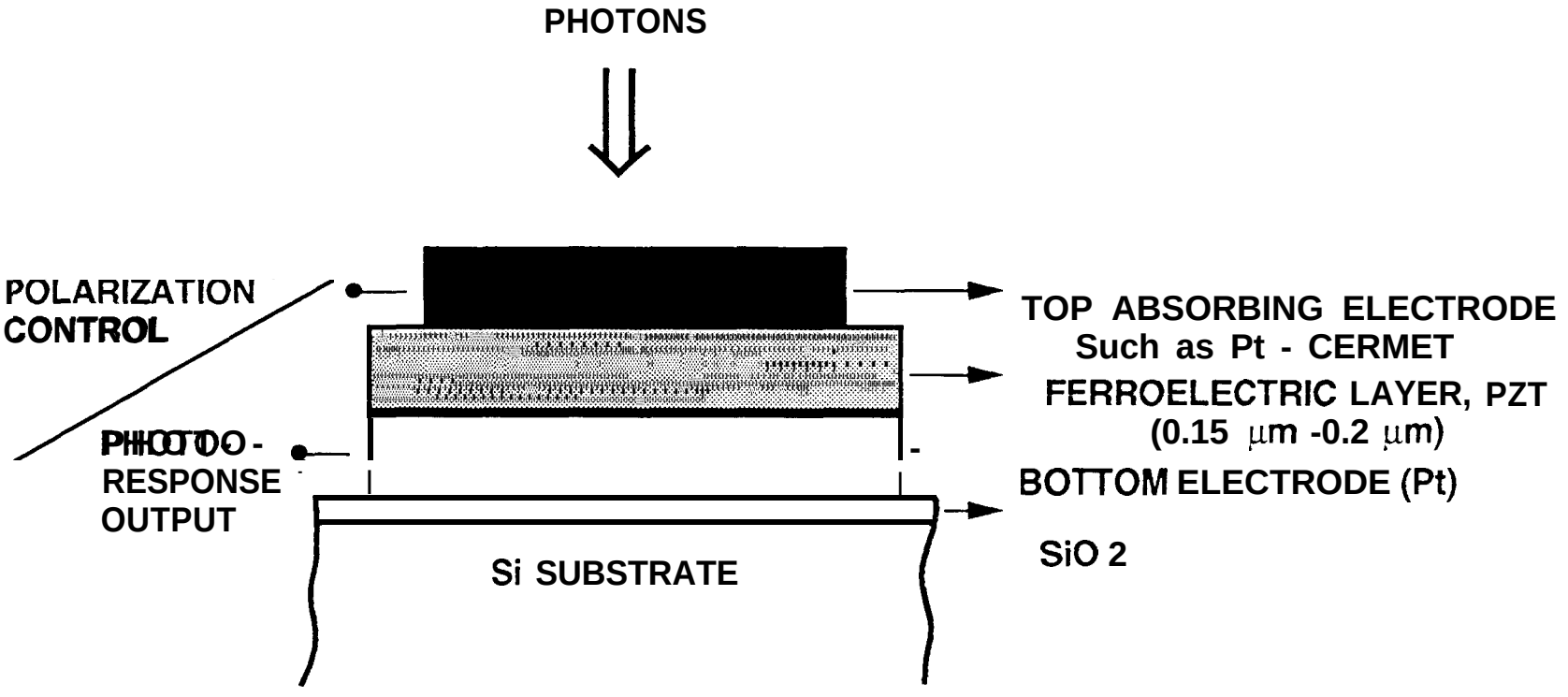

Figure 5

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OPTICALLY ADDRESSABLE THIN FILM FERROELECTRIC MEMORY CHIP PACK

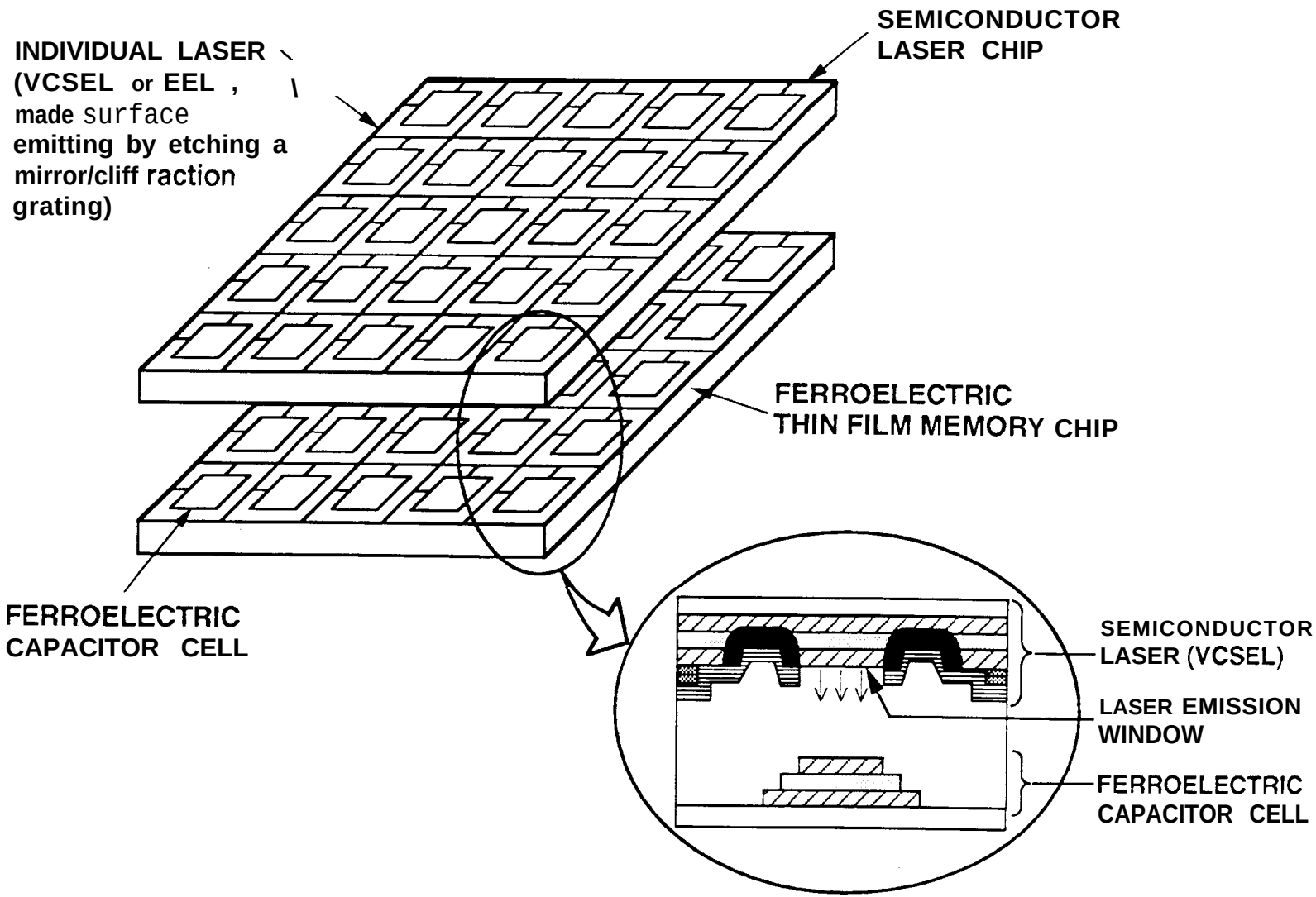

Figure 6

OPTO ELECTRONIC EFFECT - KEY OBSERVATION

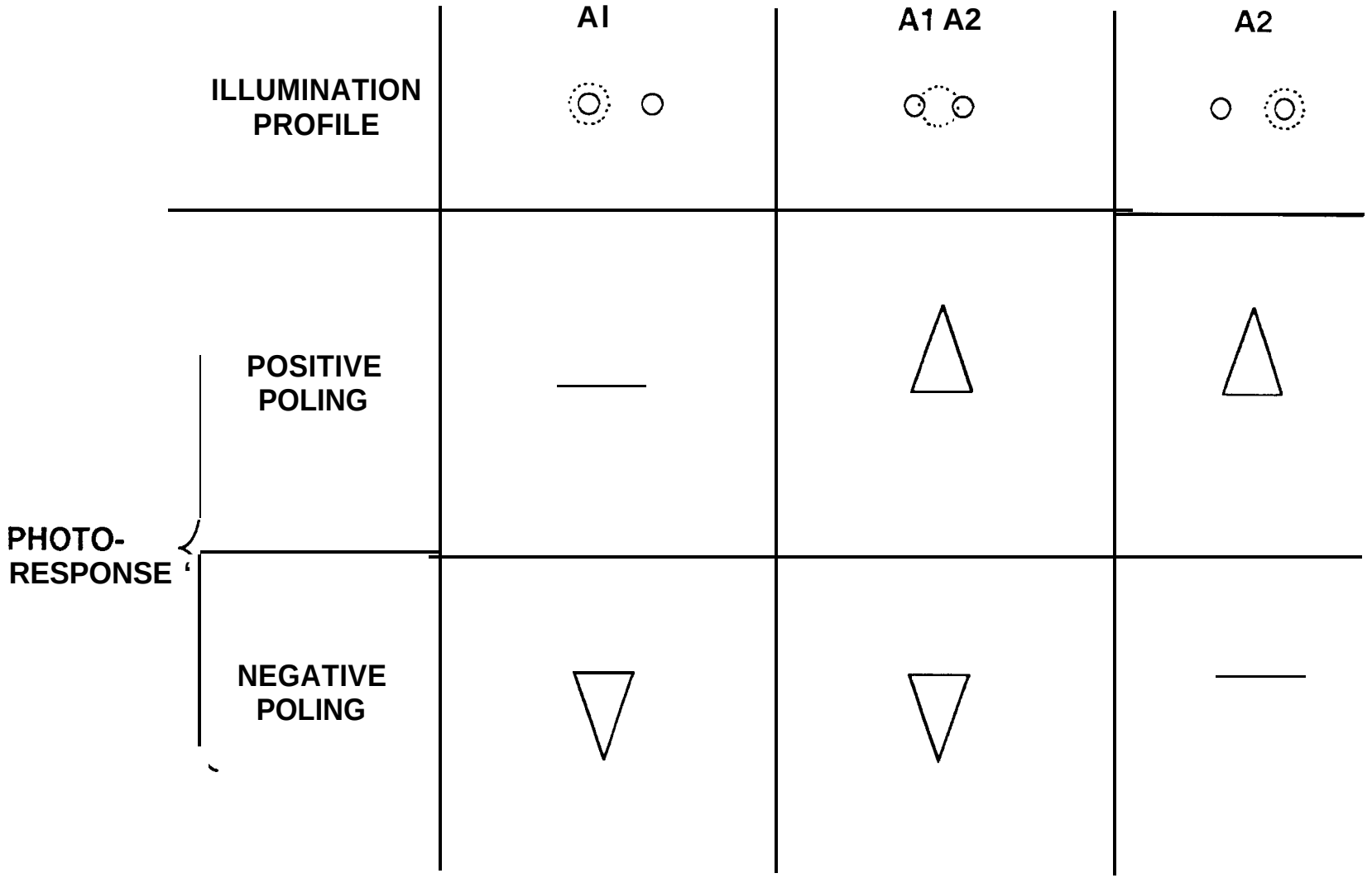

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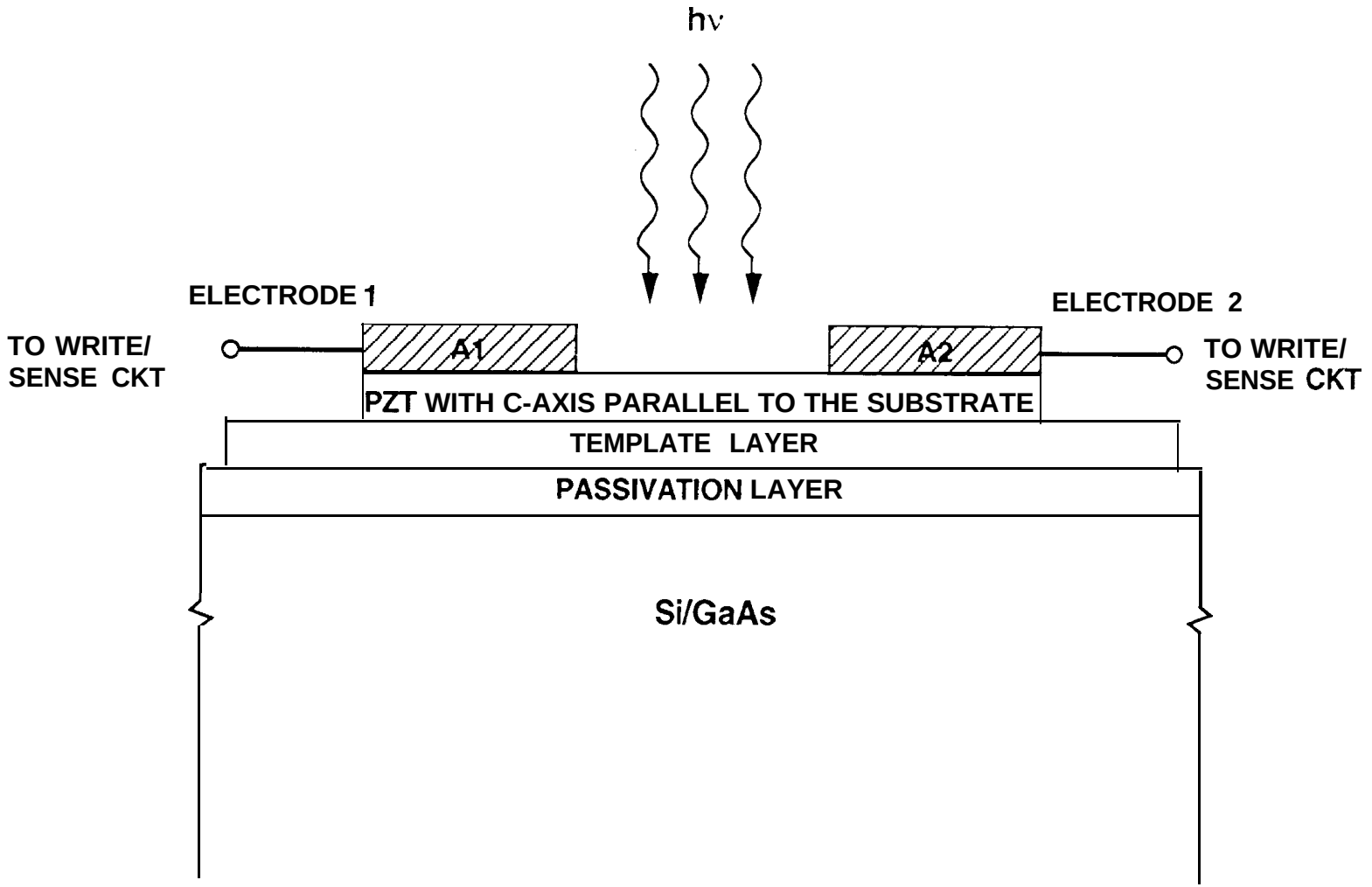
Figure 7

NEW DESIGN FOR OPTO ELECTRONIC NDRO DEVICE CONFIGURATION C



S. Thakoor
Aug' 92

Figure 8

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THIN FILM FERROELECTRIC MEMORY
OPTICALLY ADDRESSABLE NDRO

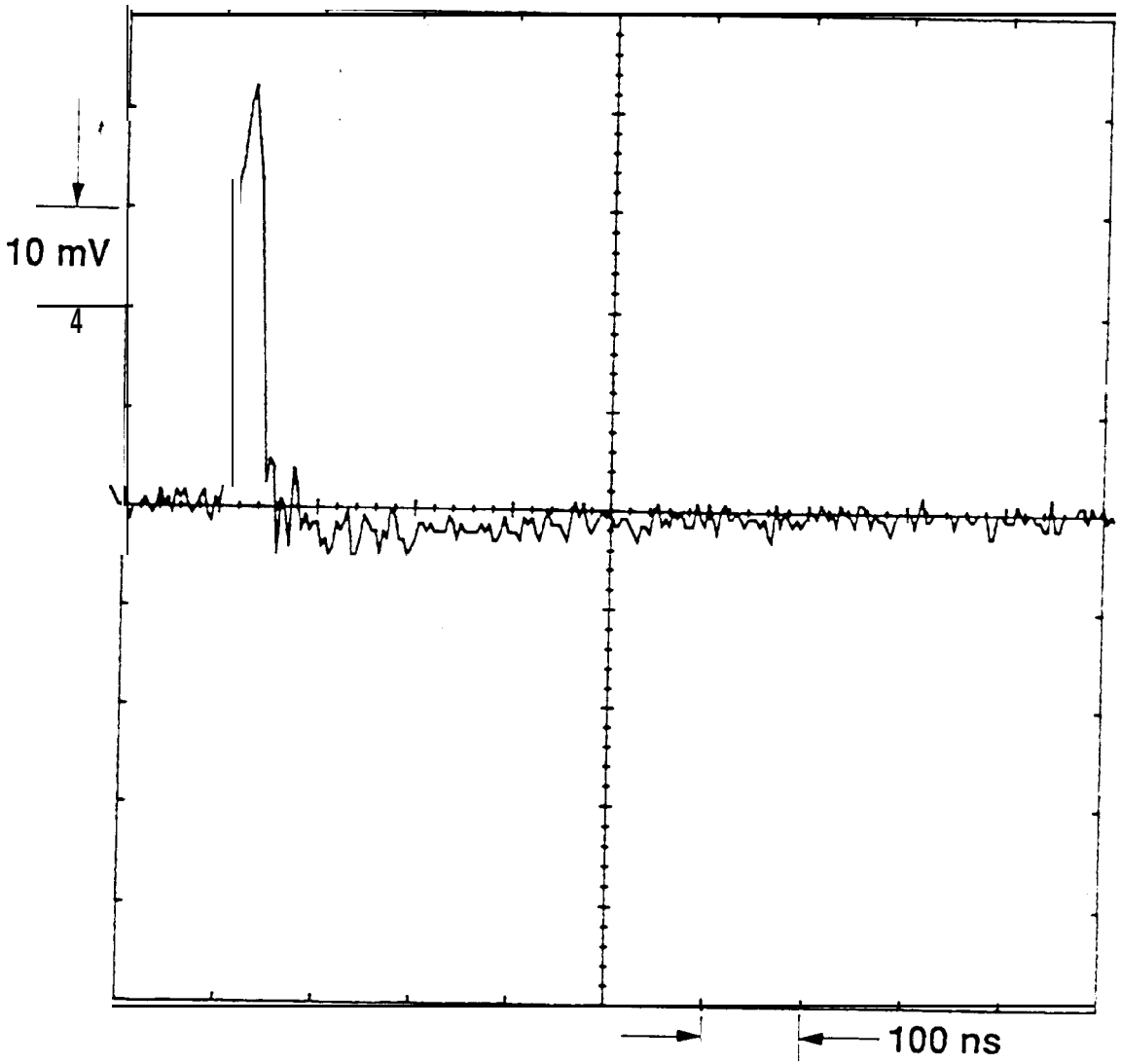

Figure 9a

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THIN FILM **FERROELECTRIC** MEMORY
OPTICALLY ADDRESSABLE NDRO

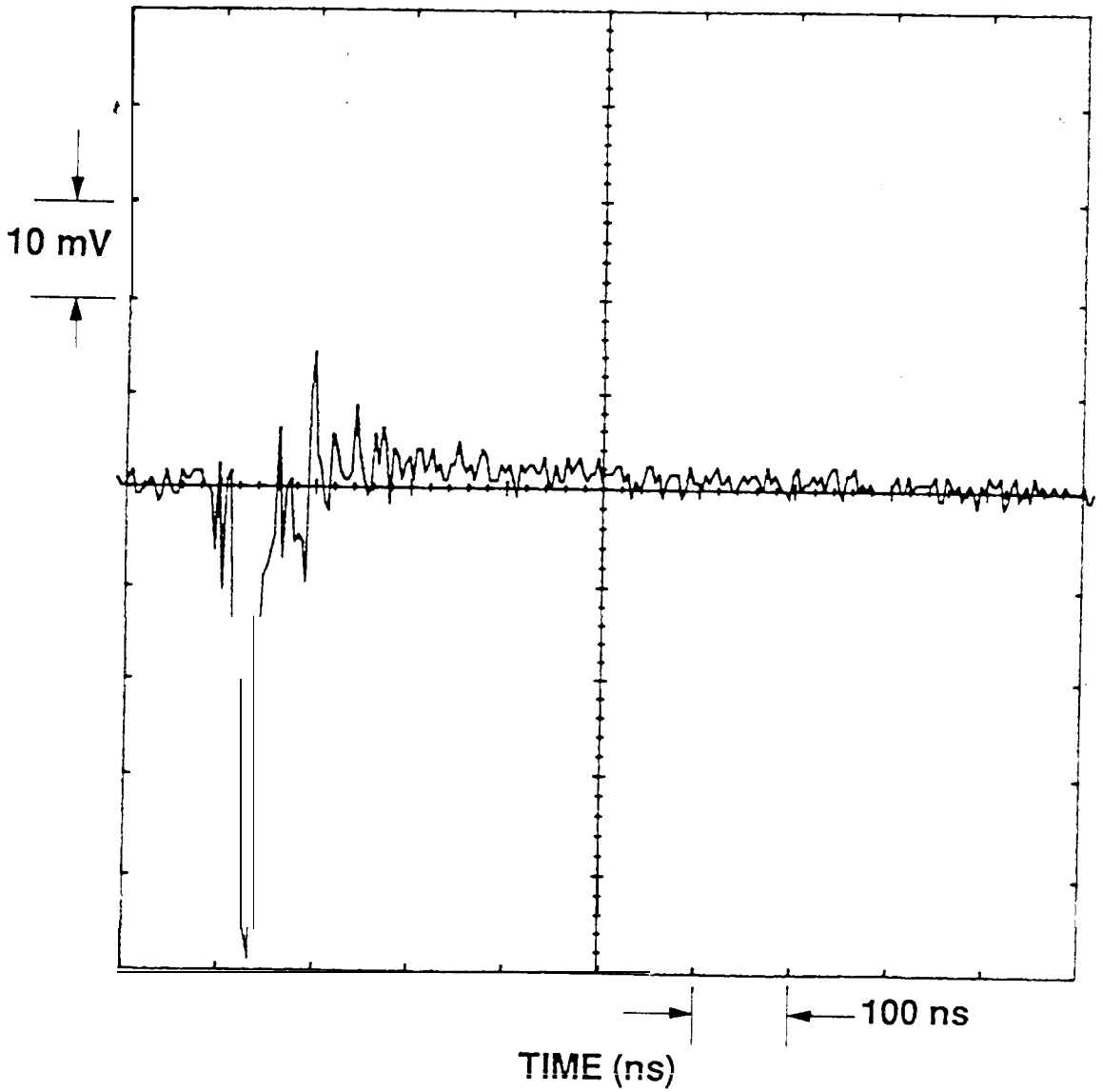
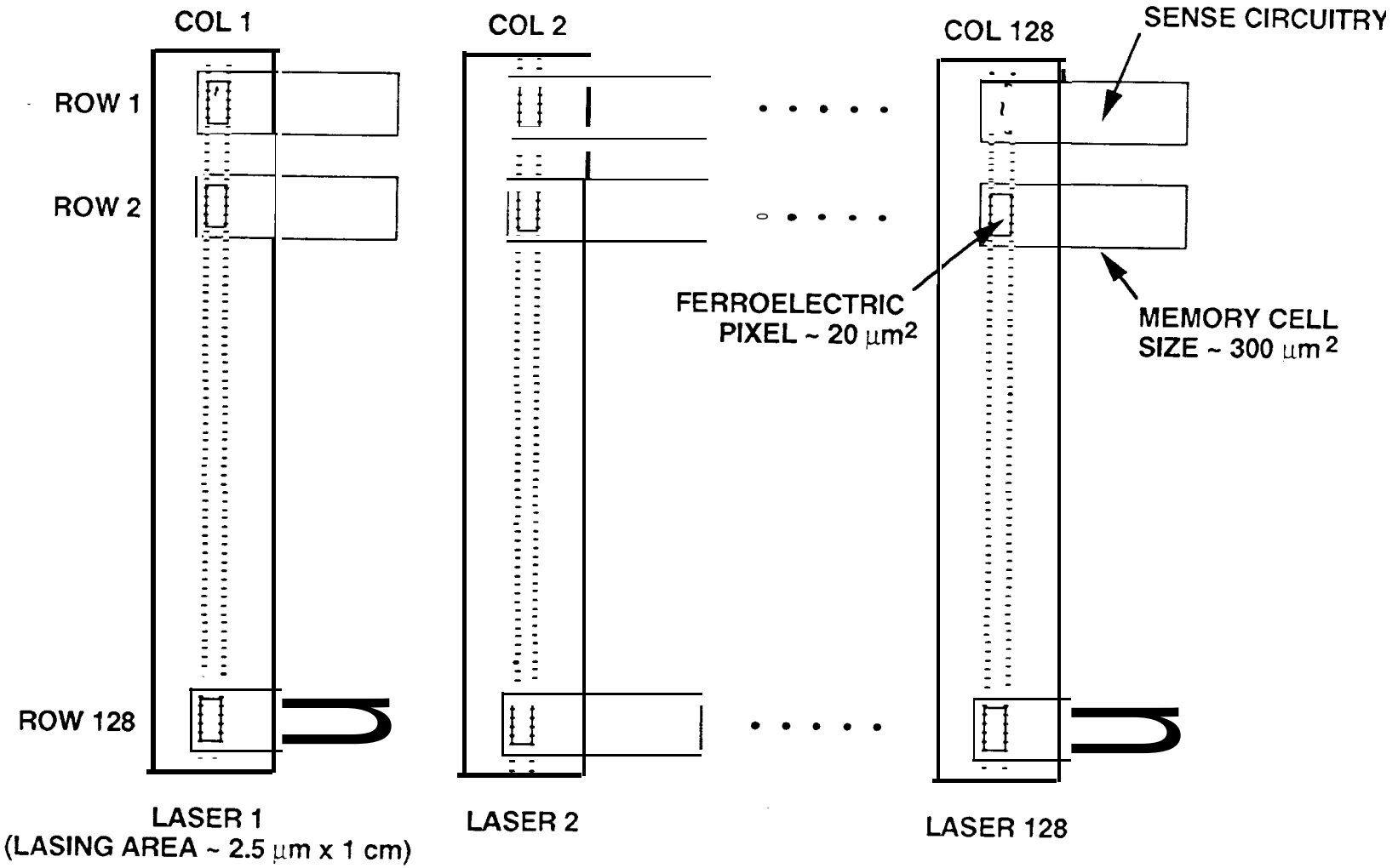


Figure 9b

LAYOUT OF 16K OPTICALLY ADDRESSABLE CHIP



S. Thakoor
July '91

Figure 10

				odu	4kx	odu		Rad
6	Taccess	(Tb+Tc+Te)	(ns)		21.33	19.58	38.33	34.25
7	Tcycle	(Taccess + Precharge)	(ns)		31.33	29.58	48.33	44.25
8	Ferro Capacitor Area		(u^2)		32.00	20.00		
						2048		

0009

34	Comparator K	(spec. unit)	5.00000E+02	5.00000E+02
35	Comparator Drive basis	(mV)	5.00000E+00	5.00000E+00
36	Comparator Null Time	(ns)	2.00000E+00	2.00000E+00
37	Column MUX Delay	(ns/column_adr_bit)	1.00000E+00	1.00000E+00
38	Precharge Time	(ns)	1.00000E+01	1.00000E+01
39	Address On Delay Time	(ns)	2.00000E+00	2.00000E+00
40	Register Setup Time	(ns)	1.00000E+00	1.00000E+00
41	Memory Cell Height (for Ferro height=0)	(u)	1.42000E+01	1.42000E+01
42	Memory Cell Width(for Ferro width=0)	(u)	1.20000E+01	1.20000E+01
43	Ferro Cell Overlap in width direction	(u)	4.00000E+00	4.00000E+00
44	Address FET Width	(u)	3.80000E+00	3.80000E+00
45				
46				
47				
48	OTHER CALC'D VALUES			
49				

8000

0000

TABLE

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OPTICALLY ADDRESSABLE FERROELECTRIC MEMORY AND ITS APPLICATIONS

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APRIL 19, 1993

PRESENTATION AT
5TH INTERNATIONAL SYMPOSIUM ON INTEGRATED FERROELECTRICS
COLORADO SPRINGS, COLORADO , APRIL 19-21, 1993

OUTLINE

- PEROVSKITES TECHNOLOGY - OVERVIEW
- WHY OPTICALLY ADDRESSABLE MEMORY.
- HIGHLIGHTS
  - HIGH SPEED
  - NON DESTRUCTIVE
  - BROAD WAVELENGTH RESPONSE
- PHENOMENA
- APPLICATIONS
- CONCLUSIONS

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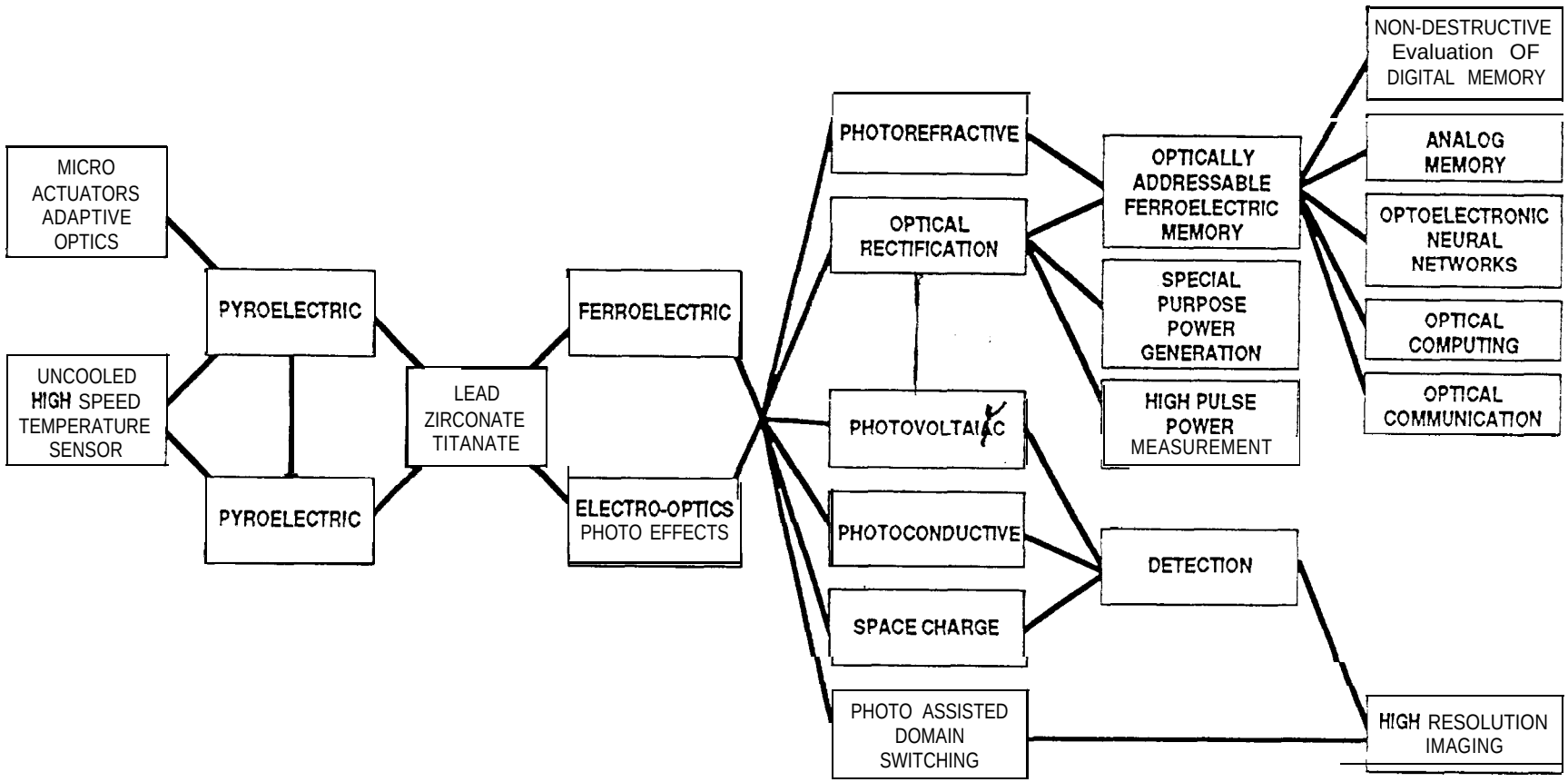
PHOTORESPONSE FROM THE LEAD ZIRCONATE TITANATE **(PZT) MATERIAL SYSTEM**



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WHY OPTICALLY ADDRESSABLE FERROELECTRIC MEMORY WITH NDRO

.PROBLEMS WITH DRO

- **destructive, demands refresh, shortens memory life**
- **CHOICE OF REFERENCE IS NON-TRIVIAL**
- **SENSITIVITY TO BIT UPSET AT REFRESH**

- *NDRO is the answer*

.PROBLEMS WITH ELECTRICAL NDRO

- FERROELECTRIC **FIELD EFFECT TRANSISTOR**
  - **relies on modulation of source to drain current across a variable resistance semiconductor channel or thin film**
  - **more complex - three terminal structure**
- **REQUIRES OPTIMIZATION OF NEW SEMICONDUCTOR** FERROELECTRIC INTERFACE
  - **injected space charge may contribute to spurious modulation**
  - **leakage associated with interface**

- *OPTICAL NDRO IS THE SOL UTION*

JPL ADVANTAGES OF OPTICALLY ADDRESSABLE FERROELECTRIC MEMORY

- **NON-DESTRUCTIVE READOUT**
- **HIGH SPEED INTERACTIVE ACCESS ($\leq$ 35 ns)**
- DIRECT ACCESS WITH OPTICS
- OPTICAL COMPUTING
- CYCLABILITY **TO** $\geq 10^{15}$ cycles
- BROAD WAVELENGTH RESPONSE **(0.5 μ - 5p)**

HIGH SPEED, OPTICAL NON DESTRUCTIVE EVALUATION OF FERROELECTRIC MEMORY

- A MANUFACTURING AID FOR FERRO NUM.

OPTICAL NDE	CURRENT ELECTRICAL TESING
• HIGH SPEED (~10ns)	• LOWER SPEEDS (~100ns)
• PARALLEL BLOCK ADDRESSING.	
NON DESTRUCTIVE TESTING ~~OF UNAGED DEVICE~~	DESTRUCTIVE ~~AGING CANNOT~~
• NO FATIGUE	• FATIGUE DUE TO POLARISATION SWITCHING CANNOT BE AVOIDED
• TRUE TEST OF AGING	• AGING TEST BASED ON

COMPARISON FERROELECTRIC AND SEED DEVICE.

FERROELECTRIC	SEED.
ANALOG MEMORY WITH GRAY SCALE	BISTABLE DEVICE
• HIGH SPEED ~ns demonstrated	. SPEED LIMITING MECHANISMS • SATURATION • SPACE CHARGE FIELD.
• BAND GAP INDEPENDENT	BAND GAP DEPENDENT
• BROAD WAVELENGTH RESPONSE	NARROW RANGE OF OPERATION . TUNED DEVICE

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WHERE ELSE THIS TECHNOLOGY WILL LEAD

. MASSIVELY PARALLEL READOUT

EXTREMELY IMPORTANT FOR OPTICAL COMPUTING AND PARALLEL PROCESSING

- direct interface with optics
- photocurrent = incident illumination x memory
- fast real time processing ~ 10 - 100 ns

. ANALOG NON-VOLATILE MEMORY

- refresh causes quick aggregation of errors makes successful operation impossible
- NDRO IS A MUST FOR ANALOG OPERATION

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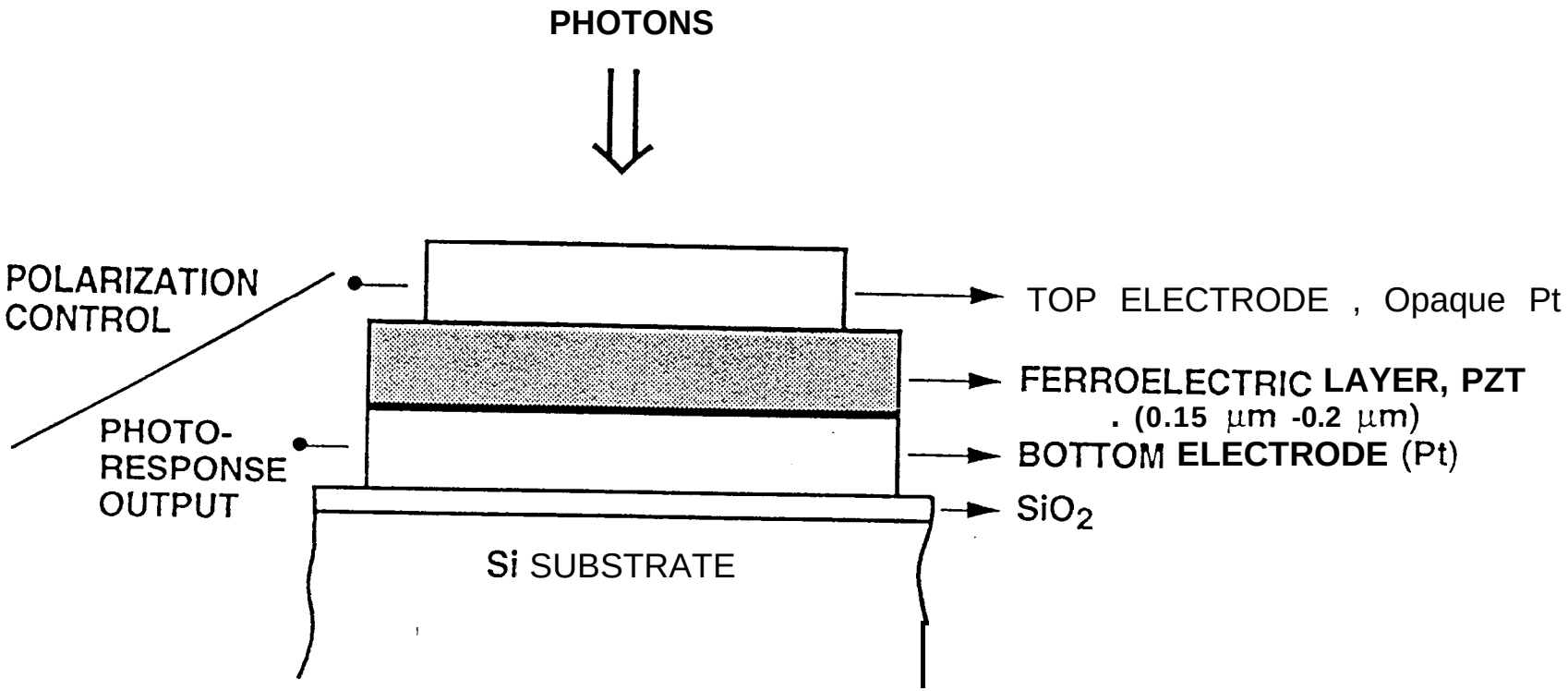
CONCEPT DEVICE CONFIGURATION A



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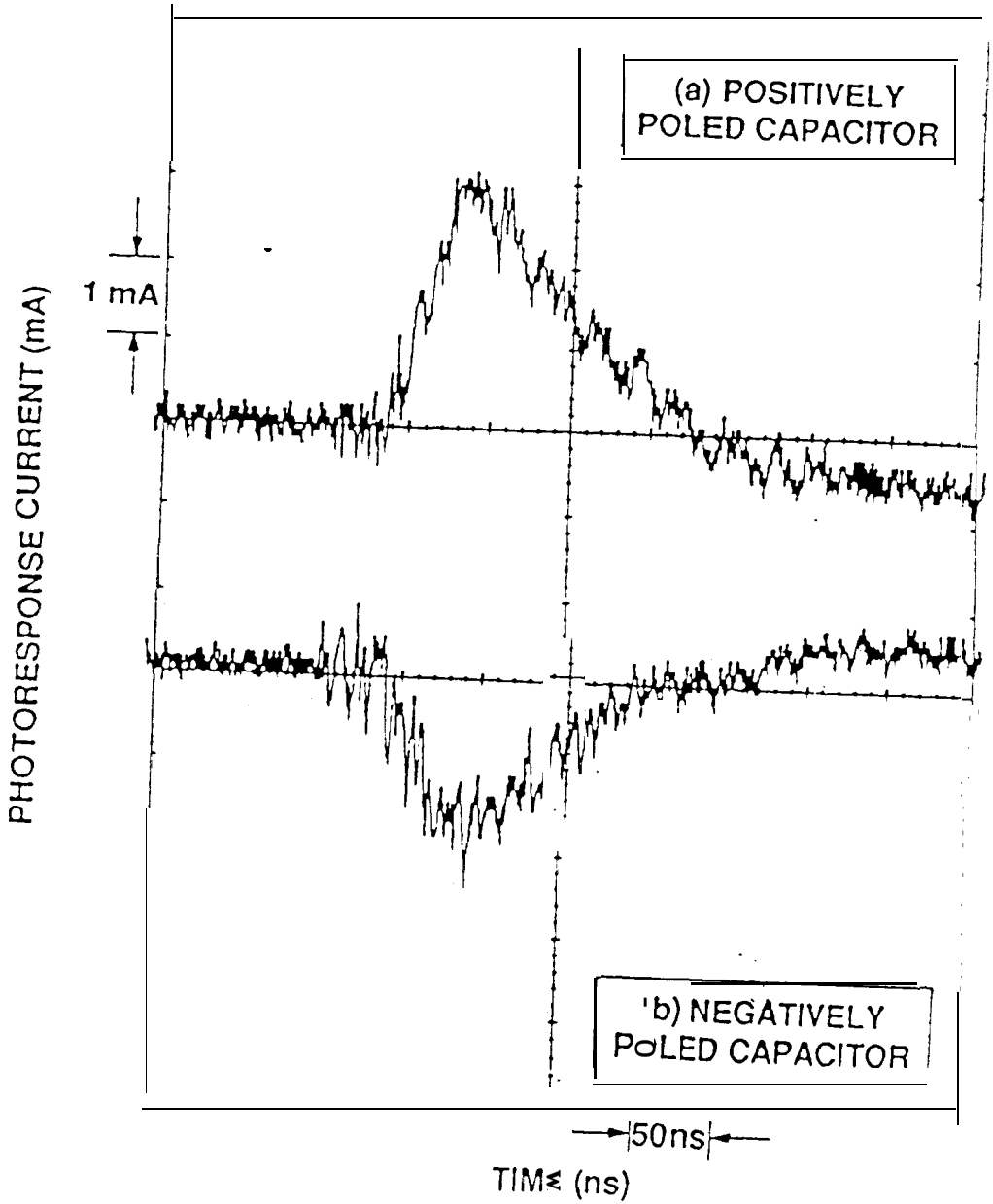
BACKGROUND

HIGH SPEED BI-DIRECTIONAL POLARIZATION DEPENDENT PHOTORESPONSE



iako et al, ISIF '92,
APL - Jun 29, 1992

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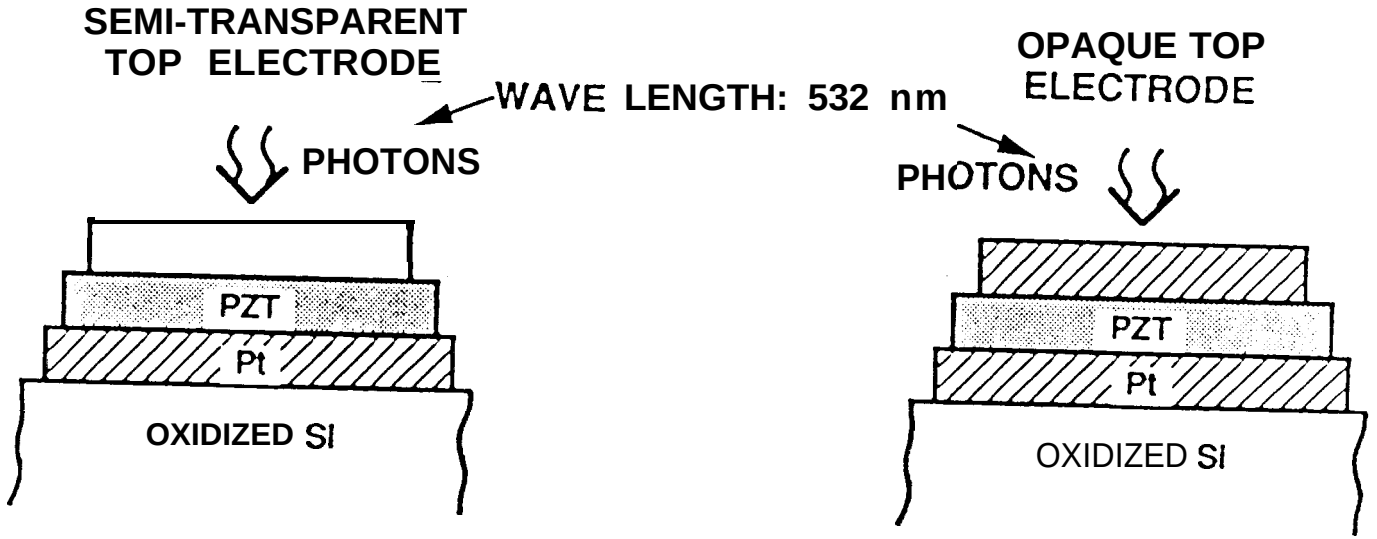
IS THE PHENOMENON THERMALLY TRIGGERED



- ASYMMETRIC RESPONSE BECAUSE OF OFFSET DUE TO POLARIZATION INDEPENDENT PHOTOVOLTAIC CURRENT

- POLARIZATION DIRECTION DEPENDENT NDRO OF MEMORY OBSERVED REPETITIVELY,

- PHOTOVOLTAIC CURRENT SUPPRESSED DUE TO OPAQUE TOP ELECTRODE. SYMMETRIC RESPONSE OBSERVED

- THERMALLY TRIGGERED PHOTORESPONSE PREDOMINANT

- POLARIZATION DIRECTION DEPENDENT NDRO OF MEMORY CLEARLY OBSERVED REPETITIVELY

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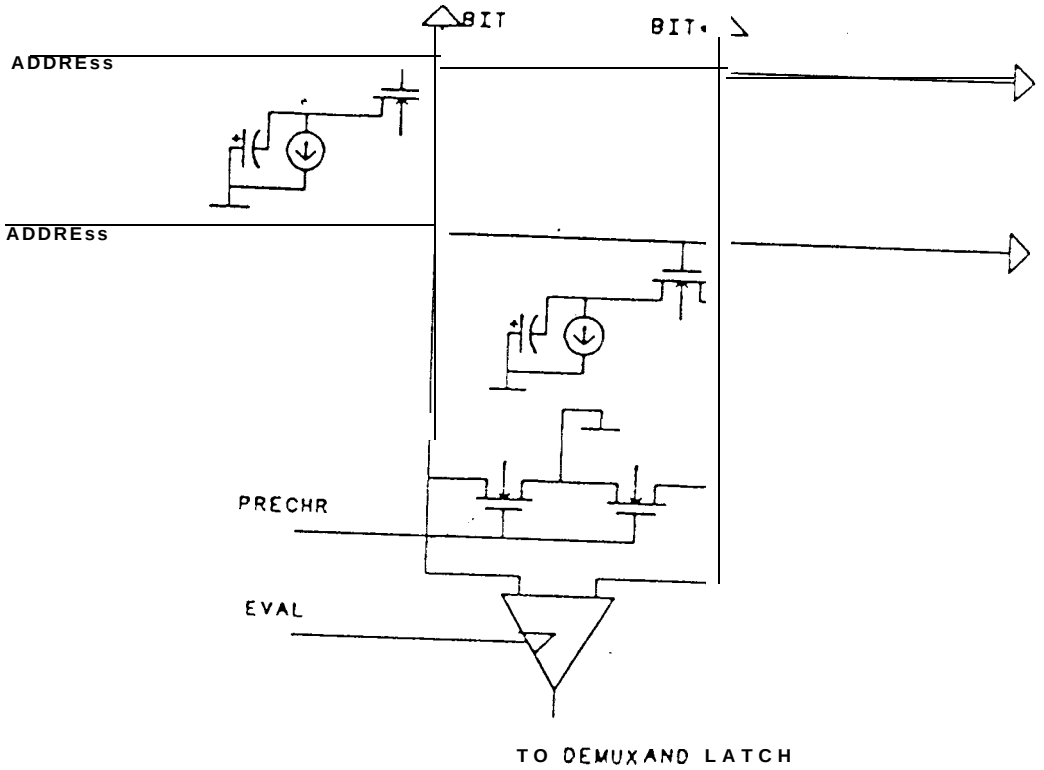
OPTICAL NDRO - VLSI IMPLEMENTALILITY



COLUMN READ FUNCTIONAL CIRCUIT

BOB NIXON and ERLEND OLSON

ACCESS TIME :

$$T_{access} = T_b + T_c + T_e$$

T_b : BIT LINE DELAY

T_c : COMPARATOR DELAY

T_e : PERIPHERAL ELECTRONIC TIMING DELAYS INCLUDE

- ADDRESSING F'CAPACITOR
- MULTIPLEXING DELAY
- SET UP TIME TO REGISTOR OUTPUT

$$T_{cycle} = T_{access} + T_{precharge}$$

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OPTICAL NDRO - VLSi IMPLEMENTABILITY

- **DEVELOPED A CONCEPTUAL** MEMORY CELL **DESIGN**
  BASED ON THE OBSERVED PHOTORESPONSE CHARACTERISTICS

- **CHOICE OF SINGLE FERRO-CAPACITOR CELL BECAME POSSIBLE DUE TO THE BI-DIRECTIONAL POLARIZATION DEPENDENT PHOTO RESPONSE**

- **ADAPTED A TYPICAL DRAM DESIGN WITHOUT REFRESH THAT UTILIZES STANDARD BALANCED BIT LINE TECHNIQUES .**

- **16 K MEMORY CHIP SIMULATION RESULTS**

	READ ACCESS TIME	READ CYCLE TIME
WITHOUT RAD HARD MARGINS	20 ns	30 ns
WITH RAD HARD MARGINS	35 ns	50 ns

- **FOR A 16 K MEMORY CHIP, THE NDRO ACCESS TIME COULD EASILY SURPASS THAT OF CONVENTIONAL DRO**

BOB NIXON and ERLEND OLSON

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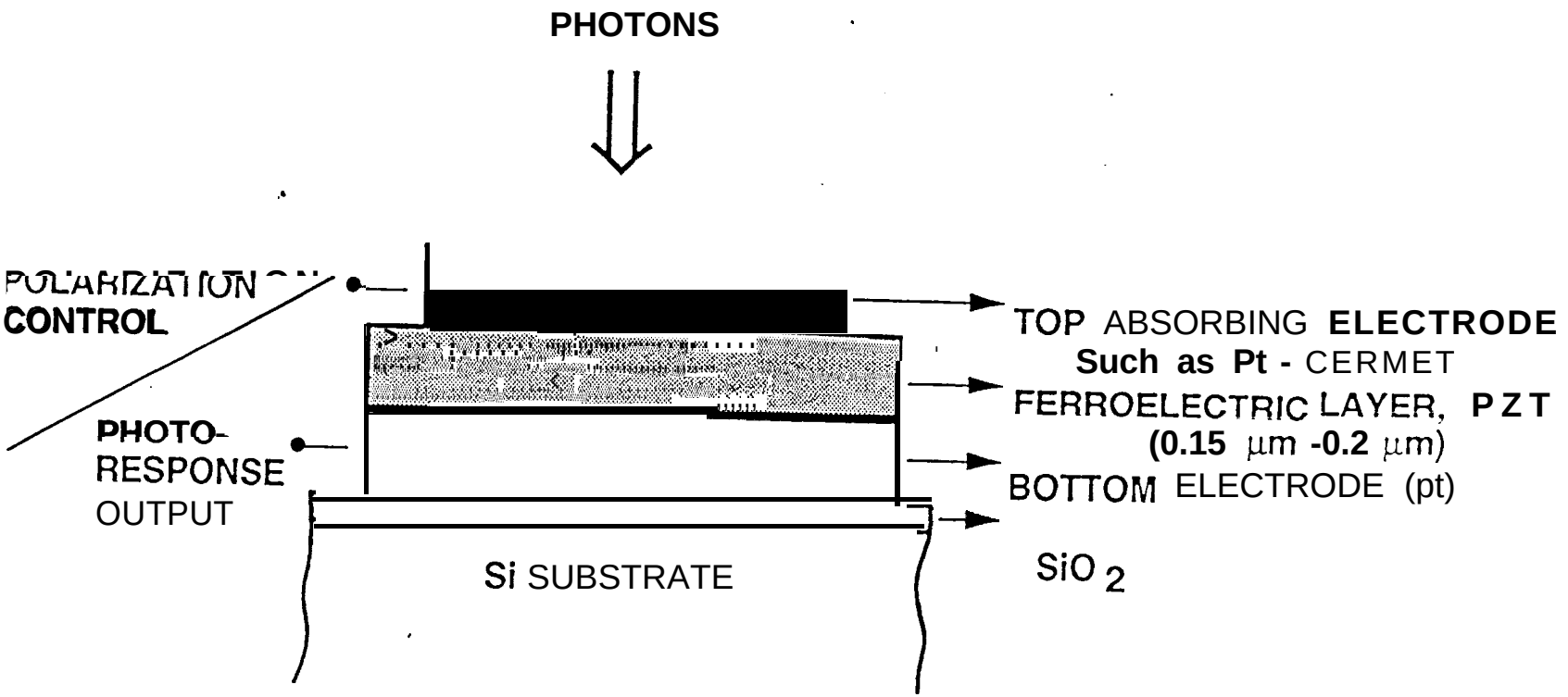
DEVICE CONFIGURATION B



IMPLEMENTATION

(CONFIG . B)

POWER REQD ~ 0·3 mW/μm^2

SEMICONDUCTOR LASERS (current-status) ~ 0·01 – 0·1 mW/μm^2

IMPLEMENTATION USING Nd YAG Laser

+

2 axis Piezo Driven Scan

(or A-O, E-O Scan)

POWER ~ 15 W

SIZE ~ 10cm × 6cm × 6cm OPTICS

10 cm × 10 cm × 10 cm ELECTRONICS

SPEED

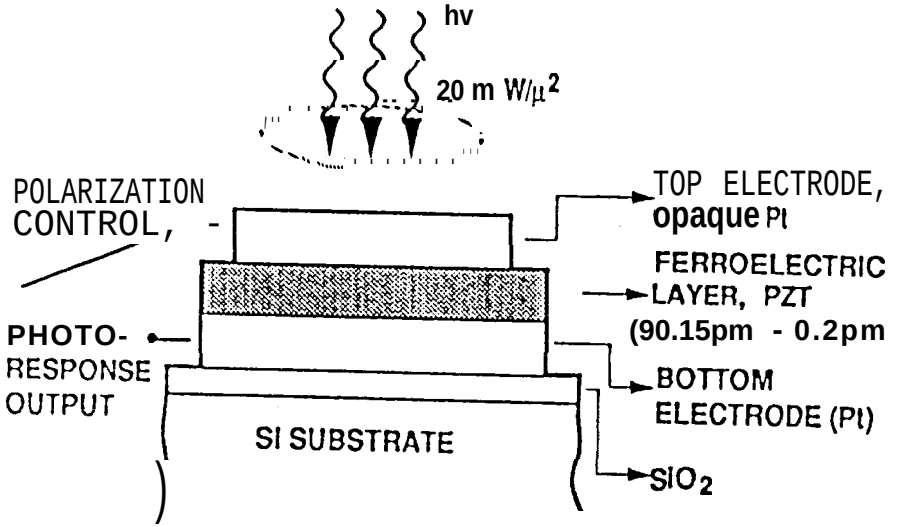
BIT ACCESS ~ 100 ns

CYCLE ~ 1 μs

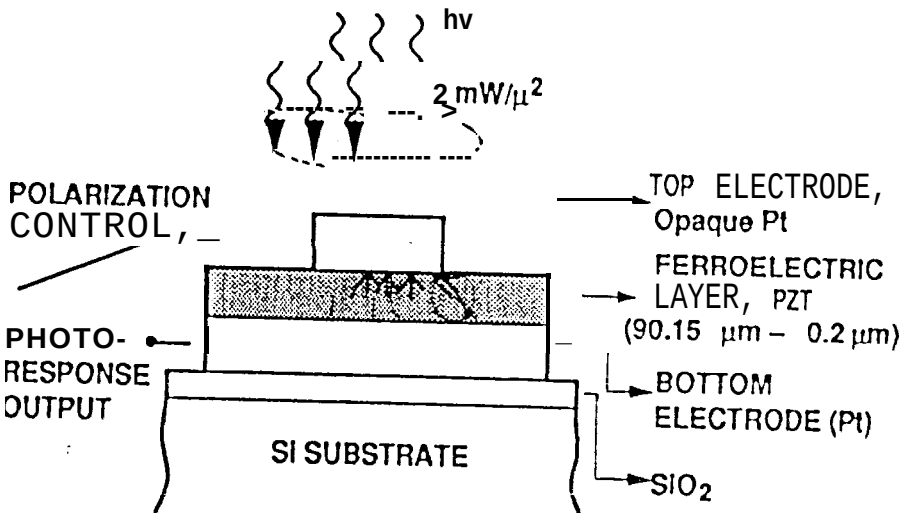
PHOTORESPONSE **AT HIGH SPEEDS, HIGH ENERGY**

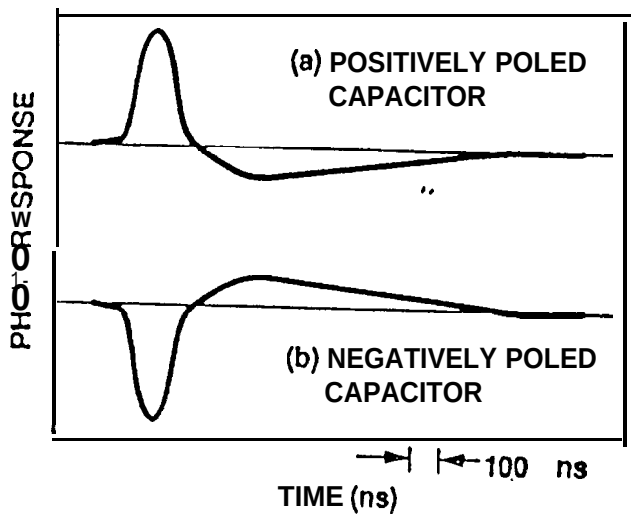
$\lambda \sim 532$ nm

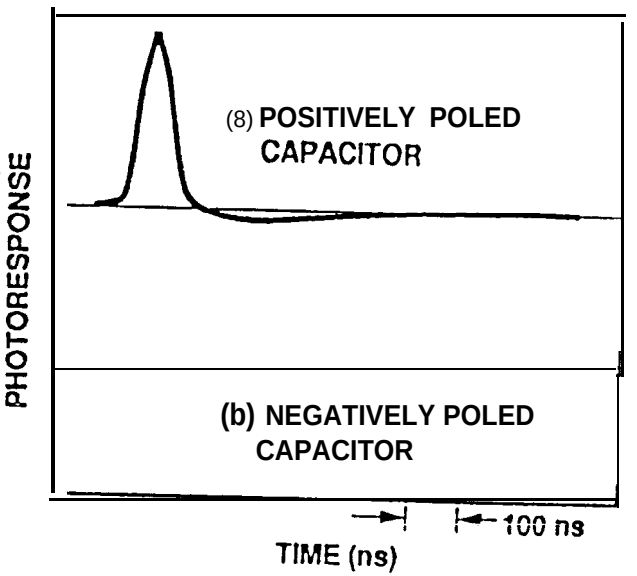
THERMALLY TRIGGERED RESPONSE



OPTO ELECTRONIC RESPONSE







JPL COMPARISON OF THERMALLY TRIGERED AND OPTOELECTRONIC RESPONSE

THERMALLY TRIGGERED RESPONSE

- **OPTICAL BEAM DIAMETER IS SMALLER THAN THE DIAMETER OF THE CAPACITOR**
- RESPONSE SPEED ~ 25ns
- **OPTICAL BEAM ENERGY** ~ 20mW/μm^2
- **RESPONSE IS BIPOLAR**
- **POLARIZATION OF INCIDENT** OPTICAL **BEAM IS** NOT SIGNIFICANT

Optoelectronic RESPONSE

- OPTICAL BEAM DIAMETER **IS LARGER THAN THE DIAMETER OF THE CAPACITOR**
- RESPONSE SPEED ~ 10ns
- **OPTICAL BEAM ENERGY** ~ 2 mW/μm^2
- **RESPONSE IS UNIPOLAR**
- **POLARIZATION OF INCIDENT** OPTICAL BEAM IS SIGNIFICANT
- **BY MOVING AROUND THE BEAM SPOT THE RESPONSE** IS SEEN TO EMERGE PRIMARILY FROM THE EDGES OF THE **CAPACITOR**

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OPTO-ELECTRONIC RESPONSE FEATURES

- RESPONSE IS DIRECTLY PROPORTIONAL TO INTENSITY
- RESPONSE SHOWS A DEPENDENCE ON THE INCIDENCE ANGLE OF THE INCIDENT LIGHT
- RESPONSE SHOWS A SIGNIFICANT DEPENCE ON THE POLARIZATION STATE OF THE INCIDENT LIGHT
- FOR PZT FILMS THAT ARE EPITAXIAL WITH C - axis PERPENDICULAR TO THE SUBSTRATE OR HAVE A PREDOMINANT (111) ORIENTATION , THE RESPONSE IS SEEN TO EMERGE PRIMARILY FROM THE EDGES OF THE FERROELECTRIC CAPACITOR

OPTO ELECTRONIC EFFECT - KEY OBSERVATION

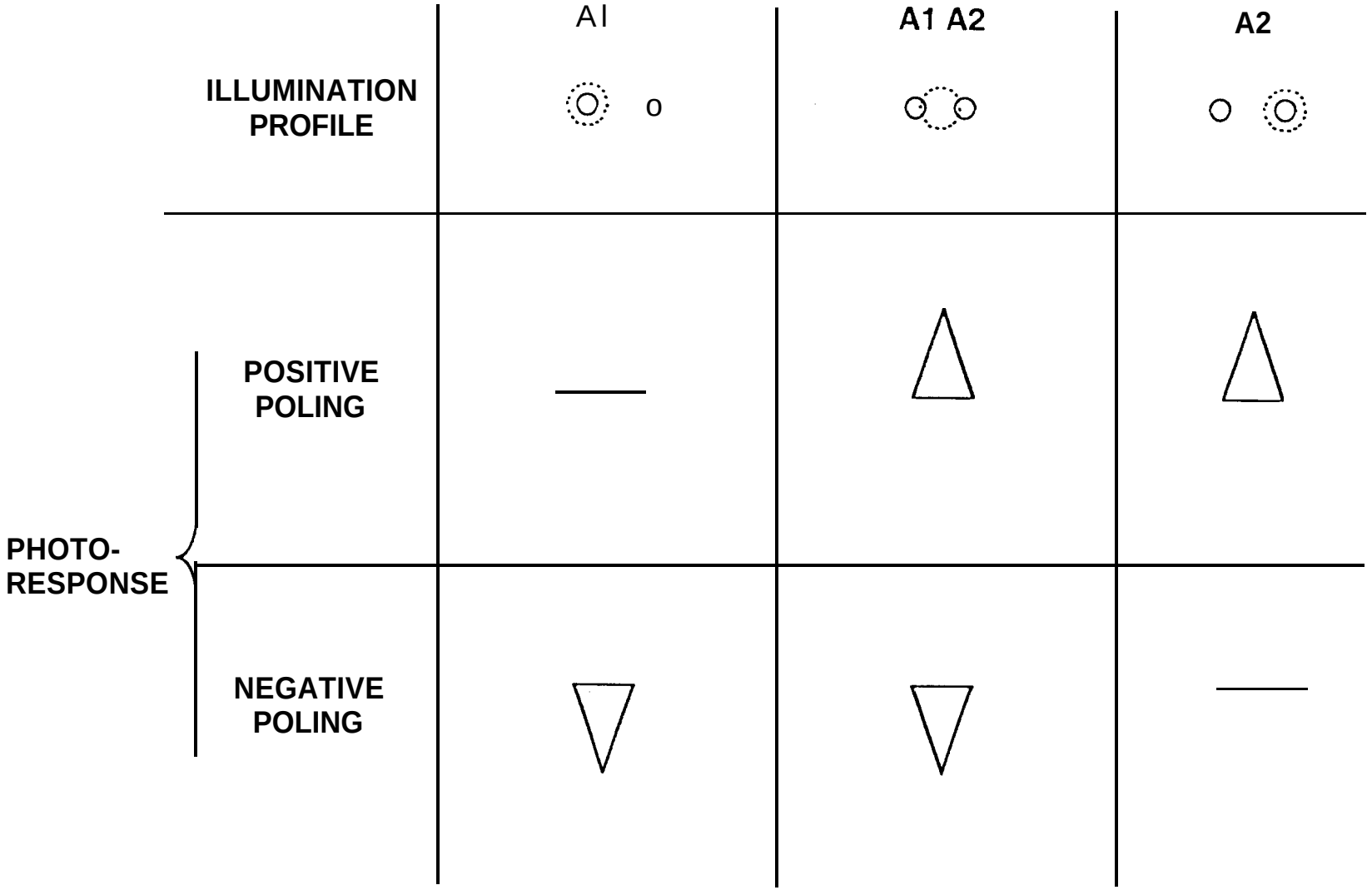

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Figure 7

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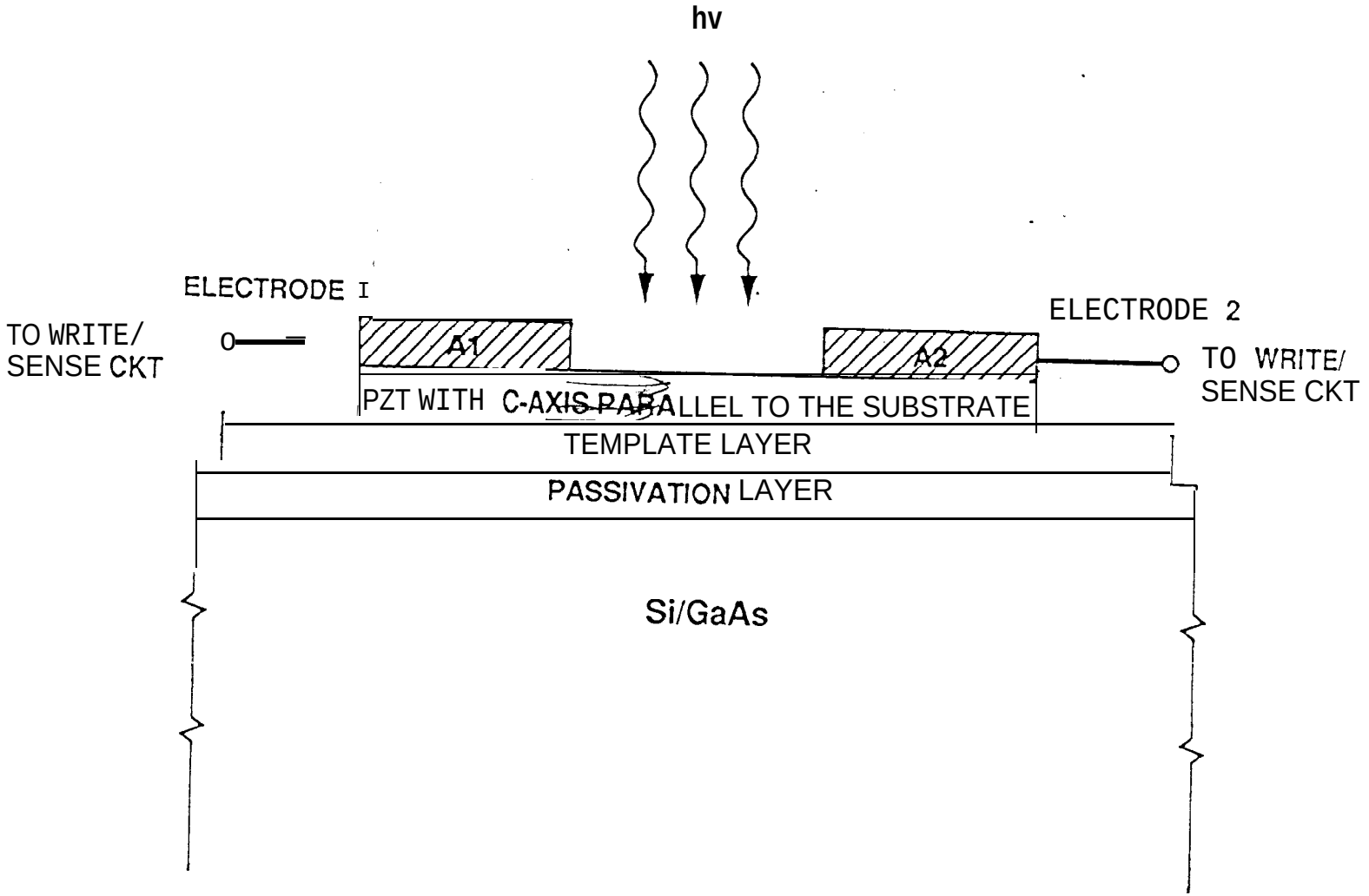
NEW DEVICE DESIGN C: OPTOELECTRONIC NDRO

KEY FEATURES

- **PZT WiTH C AXJS PARALLEL TO THE SUBSTRATE INSTEAD OF C AXIS PERPENDICULAR TO THE SUBSTRATE**
- **PLANAR CONFIGURATION INSTEAD OF SANDWICH CONFIGURATION**
- **OPTIMUM ANGLE OF INCIDENCE**
- **OPTIMUM POLARIZATION OF INCIDENT READ BEAM**

NEW DESIGN FOR OPTO ELECTRONIC NDRO



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PHOTORESPONSE MECHANISMS IN FERROELECTRICS THEIR KEY ATTRIBUTES & APPLICATIONS

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MECHANISM	INCIDENT WAVELENGTH	INCIDENT POWER	RESPONSE SPEED	APPLICATIONS
PHOTO - CONDUCTIVE PHOTOVOLTAIC SPACE CHARGE EFFECTS	DEPENDENT (bandgap related, carrier generation based)	~$\mu W/\mu^2$	~ps-ns	HIGH DEFINITION IMAGING, UV SENSING, HIGH SPEED SWITCH
OPTICAL RECTIFICATION	INDEPENDENT (interaction of the incident radiation field with the non--centrosym. material)	~$\mu W/\mu^2$ (proj.)	$\leq$ ns	NDRO, Fe DOMAIN MAP, BROAD BAND DETECTOR, HIGH SPEED cOMMUNICATION, IMAGE COMPARISON NEURAL NETS
THERMALLY TRIGGERED RESPONSE	(pyroelectric / piezoelectric response)	- (1-10) m W/μ^2	~ 10 ns *100ns	HIGH SPEED EMBEDDED TEMPERATURE CHANGE SENSOR Fe DOMAIN MAP '

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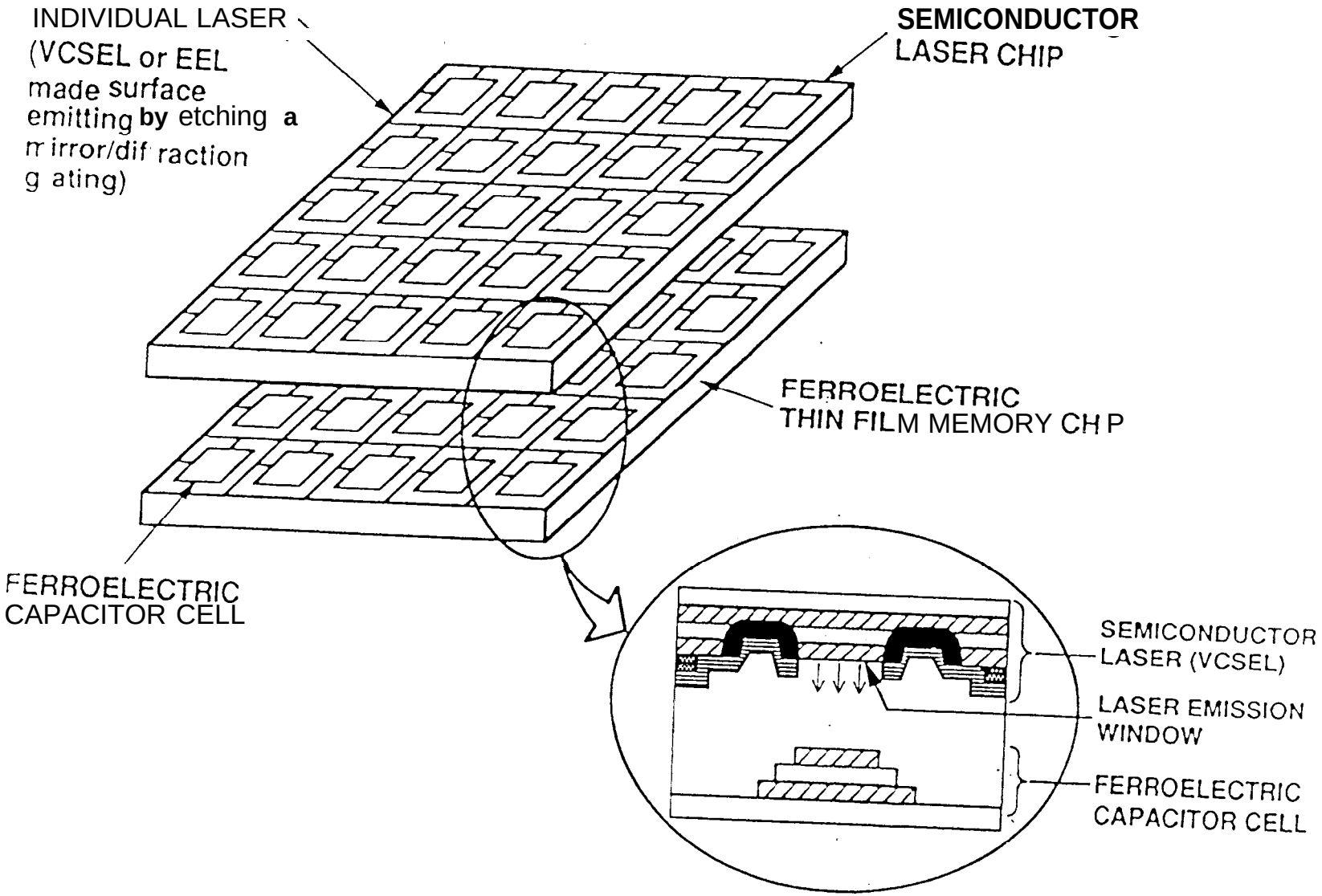
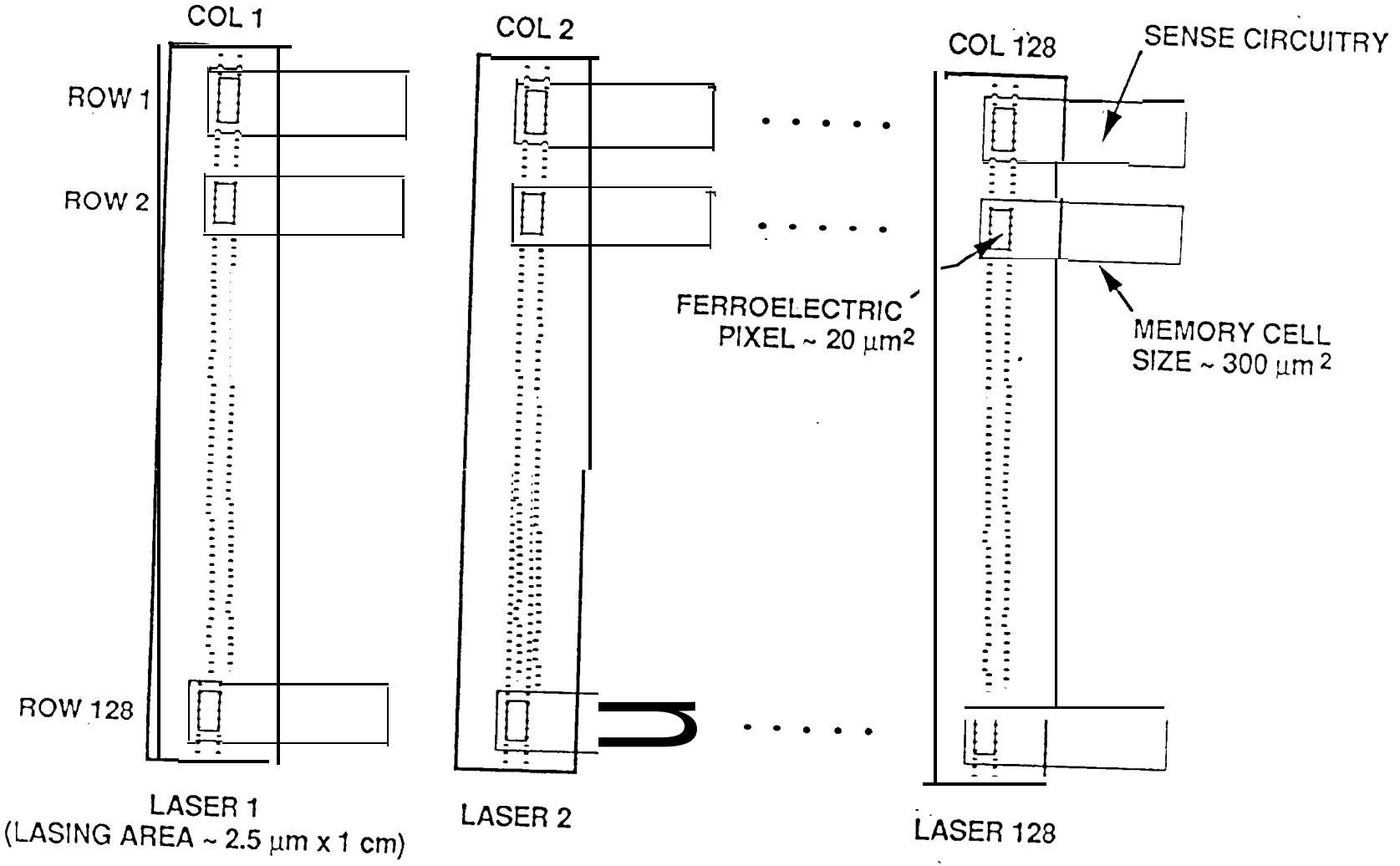
OPTICALLY ADDRESSABLE THIN FILM FERROELECTRIC MEMORY CHIP PACK



LAYOUT OF 16K OPTICALLY ADDRESSABLE CHIP



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July '91

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SIMPLIFIED OPTOELECTRONIC HEADER DETECTION/TRANSLATION INTERFACE FOR HIGH SPEED OPTICAL COMMUNICATION NETWORK

OBJECTIVE: TO DEVELOP A SIMPLIFIED OPTOELECTRONIC INTERFACE **FOR HEADER DETECTION AND TRANSLATION IN THE SWITCHING NODES OF AN ALL OPTICAL DATA PATH COMMUNICATION NETWORK WITH TERABITS/SEC CAPACITY**

BACKGROUND: **JPL** HAS INVESTIGATED THE USE OF A HIGH DENSITY WAVELENGTH **DIVISION MULTIPLEXED** (HDWDM) **FORMAT IN A MULTI-RING SHUFFLENET TOPOLOGY TO REALIZE A WIDE** AREA NETWORK (WAN) FOR INTERCONNECTION OF SUPERCOMPUTING FACILITIES AND SIMULATIONS HAVE DEMONSTRATED A POTENTIAL CAPACITY OF 1.2 TERABITS/SEC

PROBLEM: **THE OPTOELECTRONIC HEADER DETECTION/TRANSLATION IN THE SWITCHING NODES IS CURRENTLY ENVISIONED UTILIZING DISCRETE COMPONENTS AND ACCESS TO** THE ELECTRONIC MEMORY CELL **LOCATIONS IS SERIAL THUS COMPROMISING ON THE SIZE** AND THE SPEED

SOLUTION: THE FERROELECTRIC ARRAY WITH ITS DUAL ATTRIBUTES OF A MEMORY AS WELL AS A PHOTOMODULATED CURRENT RESPONSE OFFERS **AS AN IDEAL SOLUTION TO PERFORM THIS HEADER DETECTION/ TRANSLATION FUNCTION WITHIN A COMPACT INTEGRATED ARRAY**

	DISCRETE COMPONENTS	FERROELECTRIC ARRAY
SPEED	~ 10 ns	≤ 10 ns
CELL ACCESS	SERIAL	PARALLEL
POWER	~ μ W/μm^2	~ μW/μm^2 (proj.)
SIZE	requires atleast three different separate subcomponents	single integrated device "COMPACT"

NEAR FIELD, NON-INVASIVE PHOTO RESPONSE MAPPING OF POLARIZATION DOMAINS IN A FERROELECTRIC THIN FILM

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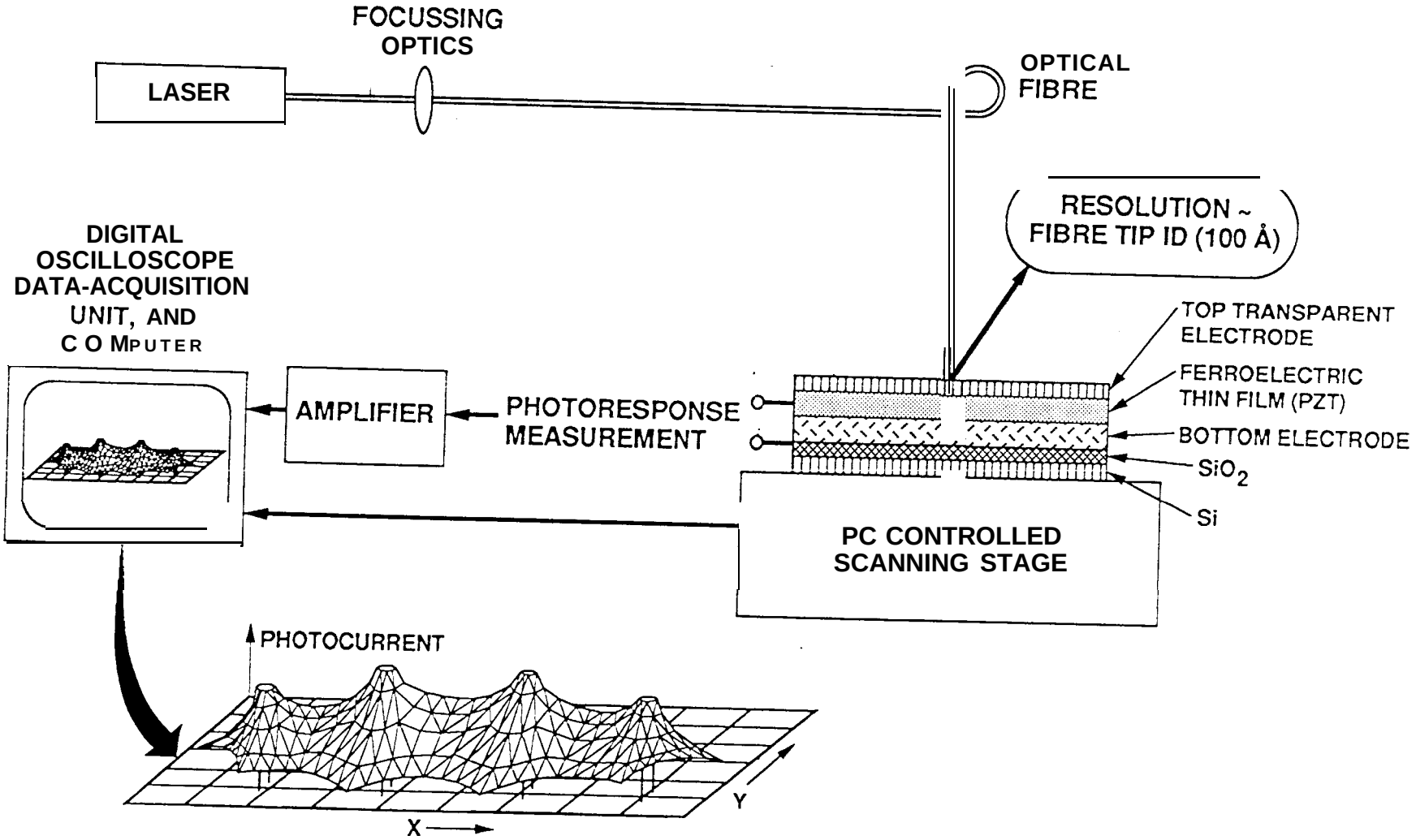

SIMULATED EXAMPLE OF SUBMICRON-RESOLUTION MAP GENERATED FROM PHOTORESPONSE DATA

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CONCLUSIONS
OPTICALLY ADDRESSABLE FERROELECTRIC MEMORY AND ITS APPLICATIONS

OPTICALLY ADDRESSABLE FERROELECTRIC MEMORY IS A VIABLE TECHNOLOGY

HIGHLIGHTS

- DEMONSTRATED **HIGH SPEED (~10ns) BIDIRECTIONAL, POLARIZATION-DEPENDENT RESPONSE AT ~mW/μm OF INCIDENT OPTICAL POWER**
- **CONCEPTUALIZATION OF A DEVICE DESIGN TO REDUCE THE REQUIREMENT OF INCIDENT OPTICAL POWER BY ORDERS OF MAGNiTUDE**
- **SIMULATION OF A 16K MEMORY CHIP WITHIN THE FRAMEWORK OF A RADIATION HARD ENVIRONMENT WITH READ ACCESS TIMES OF ≤ 35 ns & READ CYCLE TIMES OF< 50 ns**

THE VARIETY OF PHENOMENA OBTAINED WITHIN THIS ONE SINGLE MATERIAL MAKE IT AMENABLE TO A WIDE SPECTRUM OF APPLICATIONS RANGING FROM HIGH SPEED TEMPERATURE SENSING TO OPTiCAL COMPUTING

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